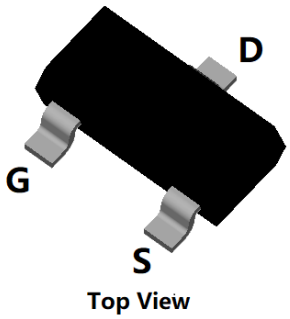
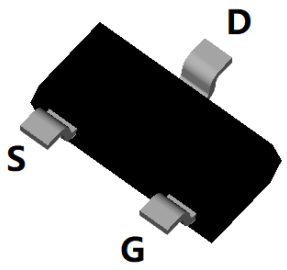
N-Channel Enhancement Mode Field Effect Transistor

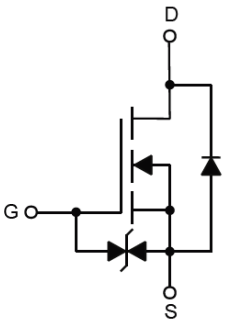


Top View



Bottom View

SOT-23



Product Summary

- V_{DS} 60V
- I_D 0.55A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜1.4Ω
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜1.5Ω
- $R_{DS(ON)}$(at V_{GS}=2.5V) ＜3.1Ω
- ESD protected up to 2.0KV (HBM)

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface：TTL/CMOS

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	60	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃, V_{GS}= 10V	I_D	-	0.55	A
		T_A=100℃, V_{GS}= 10V		-	0.34	
Pulsed Drain Current	T_A=25℃, t_p≤10μs		I_{DM}	-	1.5	
Maximum Body-Diode Continuous Current	T_A=25℃		I_S		0.55	
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	0.89	W
		T_A=100℃		-	0.35	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	150	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	140	℃/W

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
2N7002KF	F2	72KF.	3000	30000	120000	7“ reel

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA, Tj =25℃	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V, Tj =25℃	-	-	1	μA
		V_{DS}=60V, V_{GS}=0V, Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V, Tj =25℃	-	-	±10	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA, Tj =25℃	0.55	0.85	1.15	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=0.5A, Tj =25℃	-	1.07	1.4	Ω
		V_{GS}=4.5V, I_D=0.2A, Tj =25℃	-	1.1	1.5	Ω
		V_{GS}=2.5V, I_D=0.1A, Tj =25℃		1.3	3.1	Ω
Diode Forward Voltage	V_{SD}	I_S=0.5A, V_{GS}=0V, Tj =25℃	-	0.9	1.2	V
Gate Resistance	R_G	f=1MHz, Tj =25℃	-	101	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V, V_{GS}=0V, f=1MHz, Tj =25℃	-	24.3	-	pF
Output Capacitance	C_{oss}		-	5.8	-	
Reverse Transfer Capacitance	C_{rss}		-	3	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=30V, I_D=0.3A, Tj =25℃	-	1.08	-	nC
Gate-Source Charge	Q_{gs}		-	0.08	-	
Gate-Drain Charge	Q_{gd}		-	0.15	-	
Reverse Recovery Charge	Q_{rr}	I_F=0.3A, di/dt=100A/μs, V_{GS}=0V, V_R=30V, Tj =25℃	-	10	-	nC
Reverse Recovery Time	t_{rr}		-	34.6	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DS}=30V, I_D=0.3A, R_{GEN}=3Ω, Tj =25℃	-	2.9	-	ns
Turn-on Rise Time	t_r		-	2.9	-	
Turn-off Delay Time	$t_{D(off)}$		-	15.8	-	
Turn-off Fall Time	t_f		-	44.2	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A =25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the

■Typical Electrical and Thermal Characteristics Diagrams

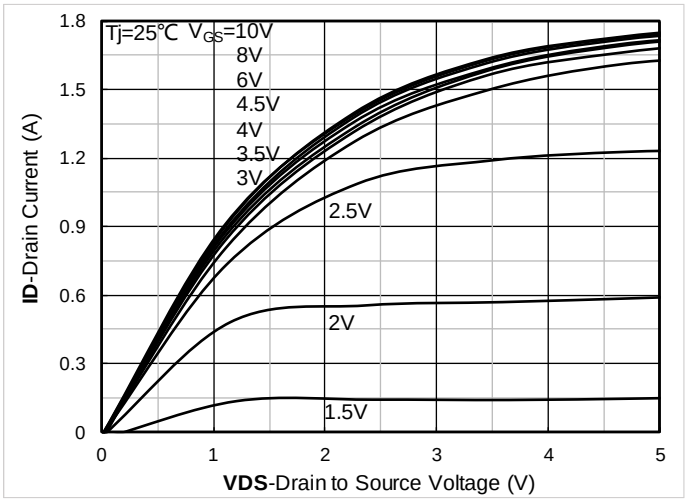


Figure 1. Output Characteristics; typical values

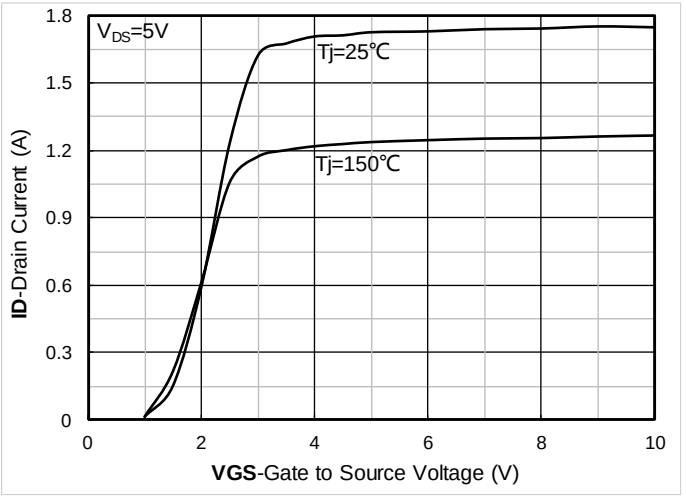


Figure 2. Transfer Characteristics; typical values

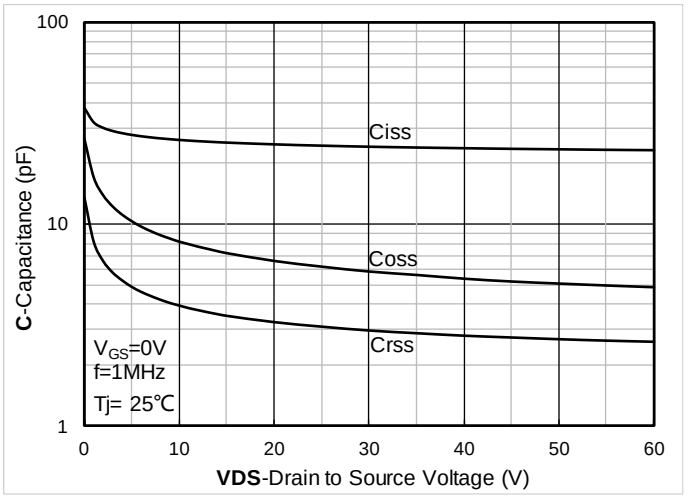


Figure 3. Capacitance Characteristics; typical values

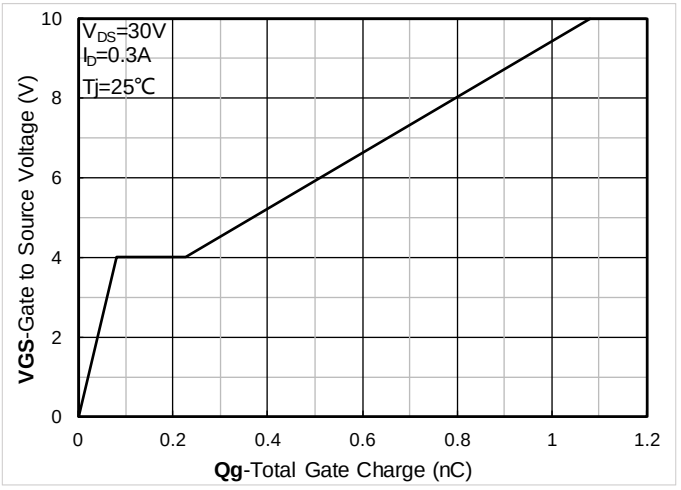


Figure 4. Gate Charge; typical values

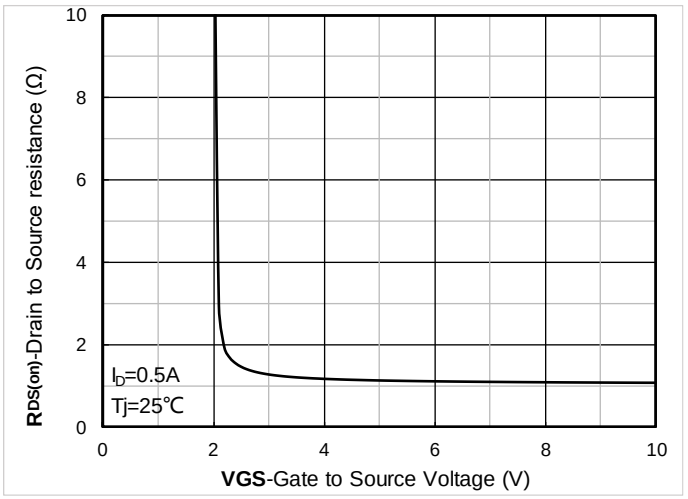


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

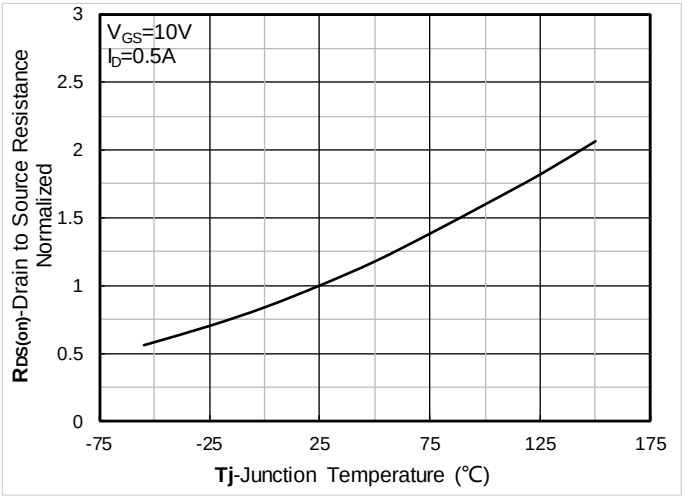


Figure 6. Normalized On-Resistance

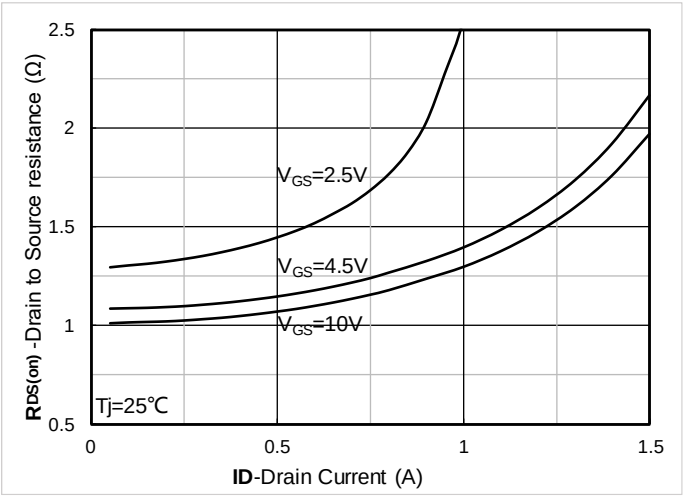


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

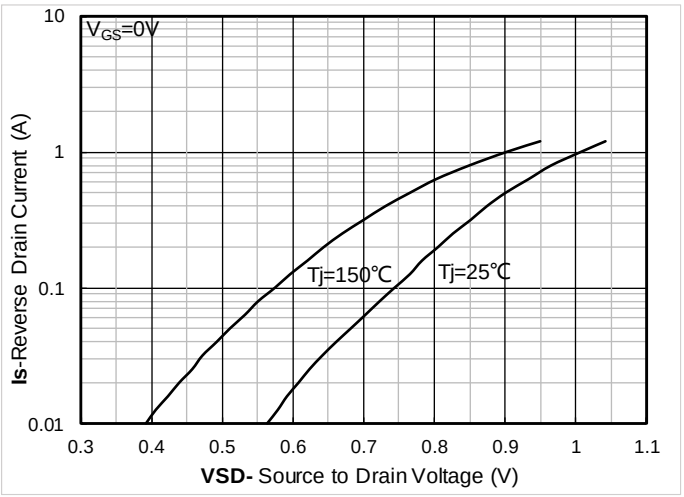


Figure 8. Forward characteristics of reverse diode; typical values

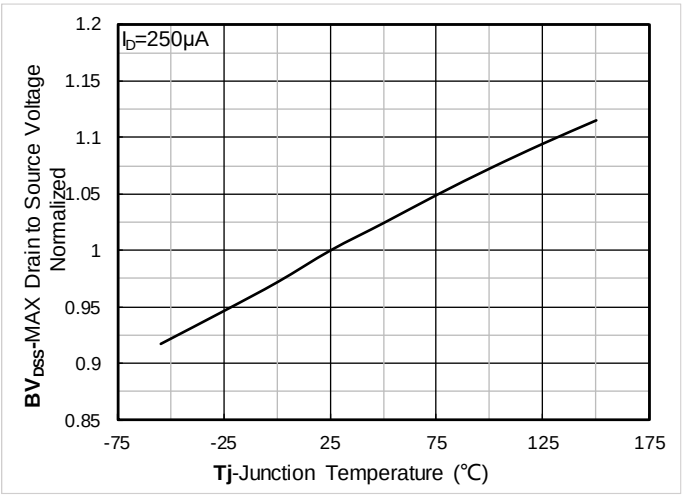


Figure 9. Normalized breakdown voltage

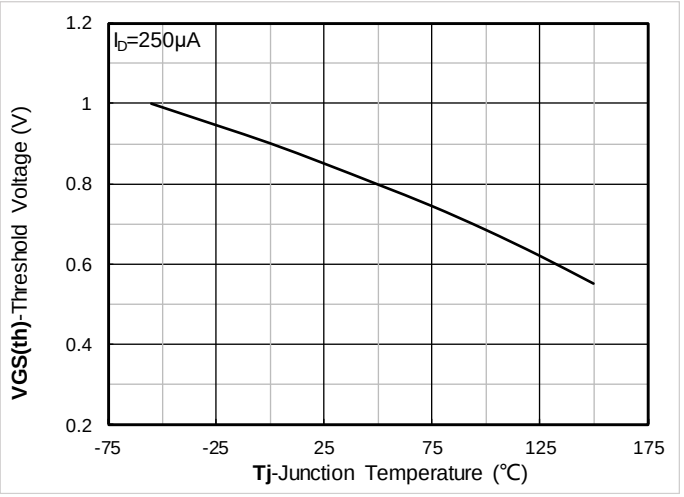


Figure 10. Gate Threshold voltage; typical values

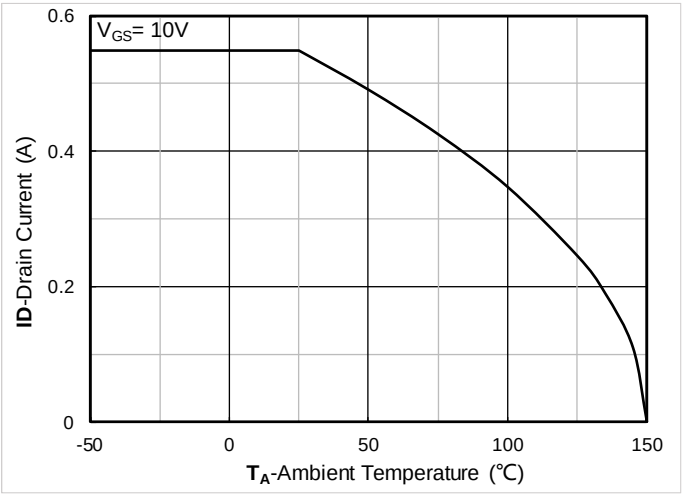


Figure 11. Current dissipation

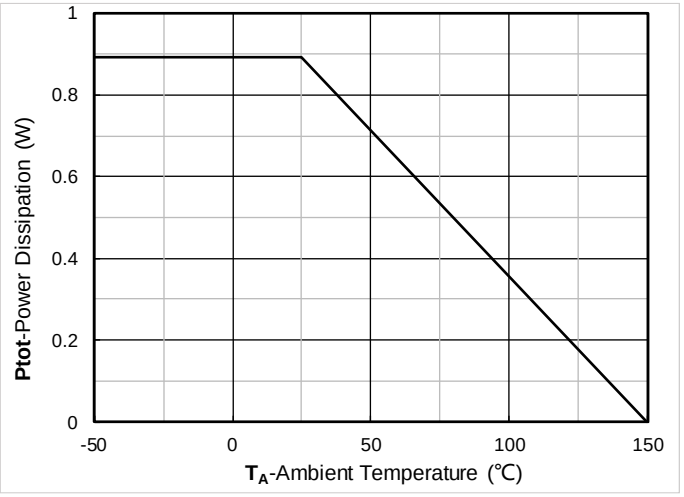


Figure 12. Power dissipation

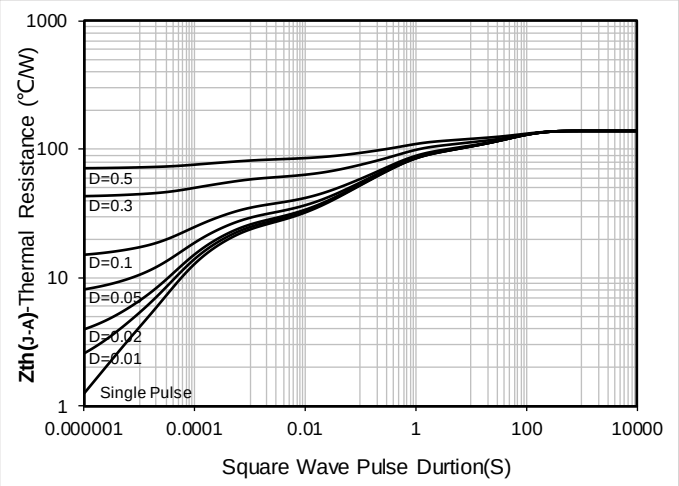


Figure 13. Maximum Transient Thermal Impedance

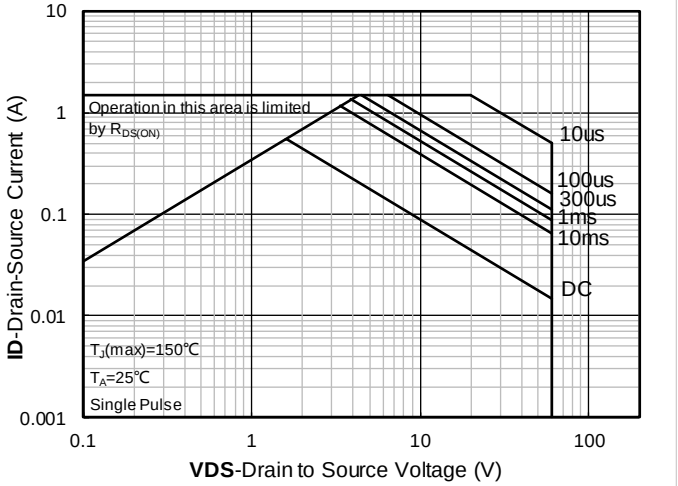
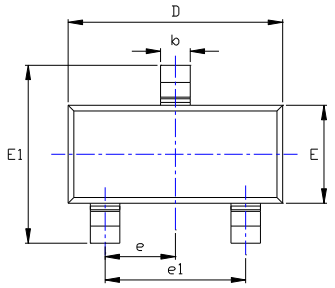
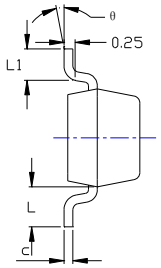


Figure 14. Safe Operation Area

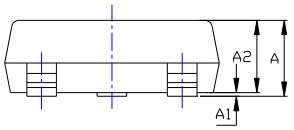
■ SOT-23 Package information



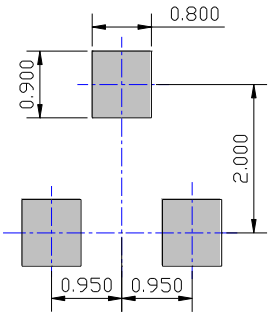
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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