# N-Channel Enhancement Mode Field Effect Transistor

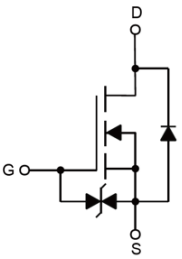


Top View




Bottom View

DFN1006-3L




## Product Summary

- $V_{DS}$ 30V
- $I_D$ 1.4A
- $R_{DS(ON)}$( at $V_{GS}$=4.5V) ＜240mΩ
- $R_{DS(ON)}$( at $V_{GS}$=2.5V) ＜300mΩ
- $R_{DS(ON)}$( at $V_{GS}$=1.8V) ＜500mΩ
- ESD Protected Up to 3.0KV (HBM)

## General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

## Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface：TTL/CMOS

## ■ Absolute Maximum Ratings ($T_A$=25℃ unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-source Voltage | | $V_{DS}$ | 30 | V |
| Gate-source Voltage | | $V_{GS}$ | ±10 | V |
| Drain Current | $T_A$=25℃ | $I_D$ | 1.4 | A |
| | $T_A$=100℃ | | 0.9 | |
| Pulsed Drain Current [A] | | $I_{DM}$ | 5 | A |
| Total Power Dissipation [B] | $T_A$=25℃ | $P_D$ | 0.8 | W |
| | $T_A$=100℃ | | 0.3 | |
| Junction and Storage Temperature Range | | $T_J$ ,$T_{STG}$ | -55～+150 | ℃ |

## ■Thermal resistance

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Thermal Resistance Junction-to-Ambient [C] | Steady-State | $R_{\theta JA}$ | 125 | 150 | ℃/W |

## ■ Ordering Information (Example)

| PREFERED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---|---|---|---|---|---|---|
| A01N03KA | F1 | 13 | 10000 | 100000 | 400000 | 7“ reel |

## ■ Electrical Characteristics ($T_J$=25℃ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$= 0V, $I_D$=250μA | 30 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=30V, $V_{GS}$=0V | - | - | 1 | μA |
| | | $V_{DS}$=30V, $V_{GS}$=0V, Tj=150℃ | - | - | 100 | |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$= ±10V, $V_{DS}$=0V | - | - | ±10 | μA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$= $V_{GS}$, $I_D$=250μA | 0.45 | 0.75 | 1 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$=4.5V, $I_D$=1.4A | - | 180 | 240 | mΩ |
| | | $V_{GS}$=2.5V, $I_D$=1.2A | - | 225 | 300 | |
| | | $V_{GS}$=1.8V, $I_D$=1.0A | - | 330 | 500 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=1.4A, $V_{GS}$=0V | - | 0.9 | 1.2 | V |
| Maximum Body-Diode Continuous Current | $I_S$ | | - | - | 1.4 | A |
| **Dynamic Parameters** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=15V, $V_{GS}$=0V, f=1MHz | - | 60 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 11 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 4 | - | |
| **Switching Parameters** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=1.4A | - | 2.4 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 0.6 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 0.4 | - | |
| Reverse Recovery Charge | $Q_{rr}$ | $I_F$=1.4A, di/dt=50A/us | - | 0.6 | - | nC |
| Reverse Recovery Time | $t_{rr}$ | | - | 8.6 | - | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}$=10V, $V_{DD}$=15V, $I_D$=1.4A $R_{GEN}$=3Ω | - | 3 | - | ns |
| Turn-on Rise Time | $t_r$ | | - | 22 | - | |
| Turn-off Delay Time | $t_{D(off)}$ | | - | 4 | - | |
| Turn-off fall Time | $t_f$ | | - | 21 | - | |

A. Repetitive rating; pulse width limited by max. junction temperature.
B. $P_d$ is based on max. junction temperature, using junction-case thermal resistance.
C. The value of $R_{\theta JA}$ is measured with the device mounted on 1 $in^2$ FR-4 board with 2oz. Copper, in the still air environment with $T_A$ =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

## ■Typical Electrical and Thermal Characteristics Diagrams

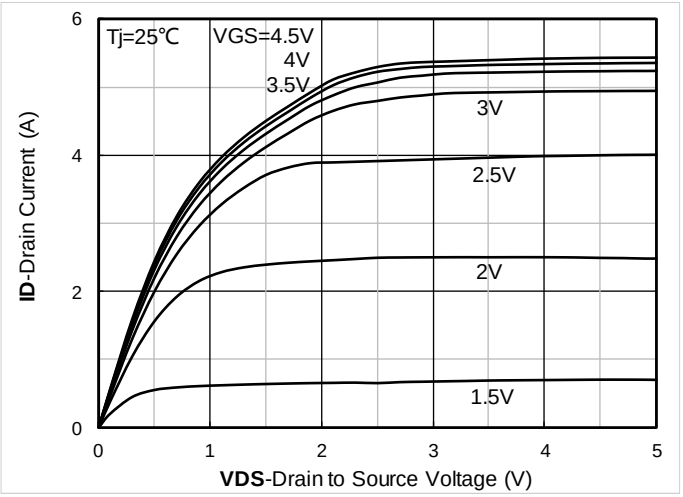



Figure 1. Output Characteristics

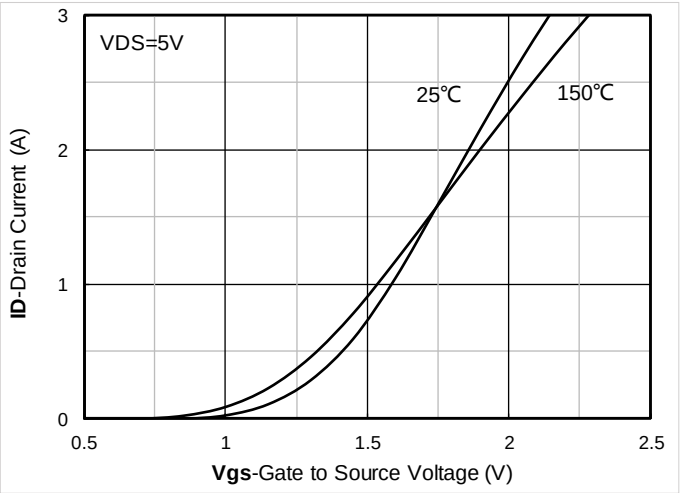



Figure 2. Transfer Characteristics

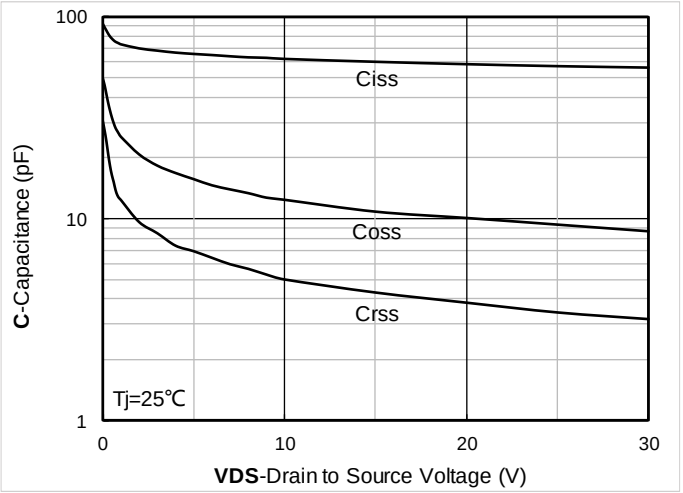



Figure 3. Capacitance Characteristics

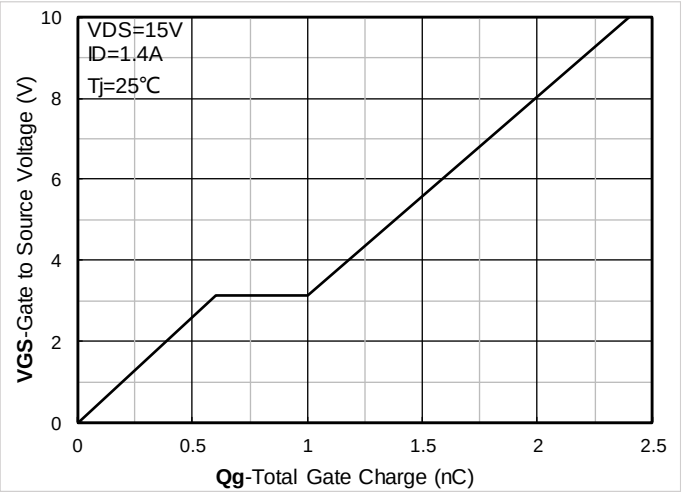
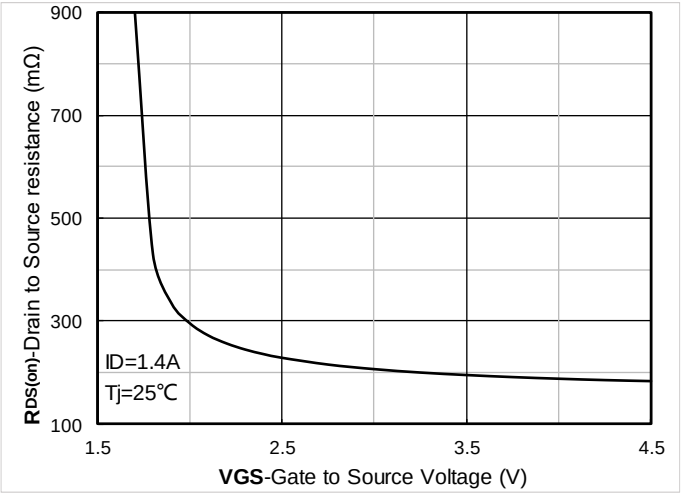
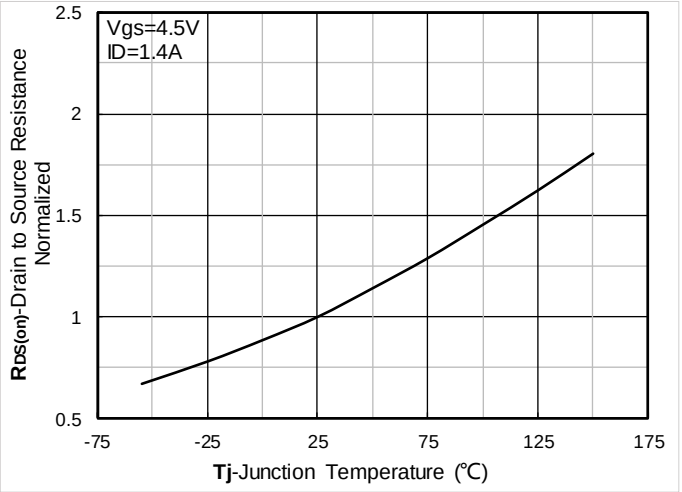



Figure 4. Gate Charge



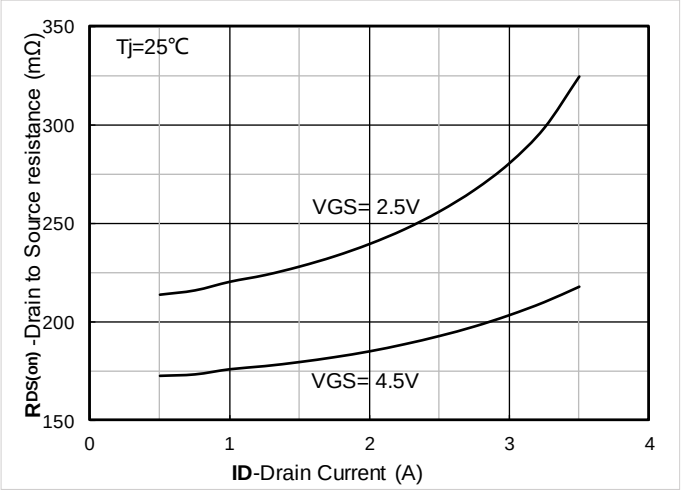



Figure 7. $R_{DS(on)}$ VS Drain Current

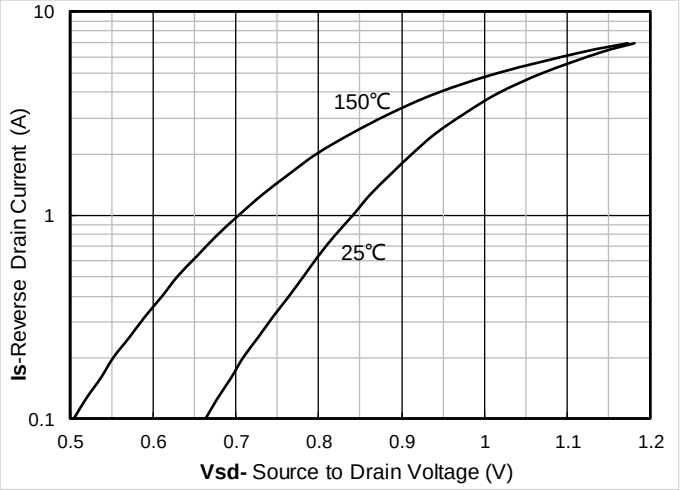



Figure 8. Forward characteristics of reverse diode

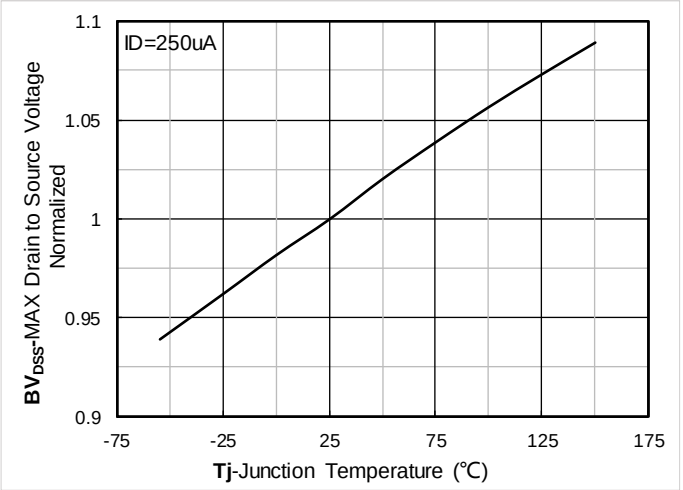



Figure 9. Normalized breakdown voltage

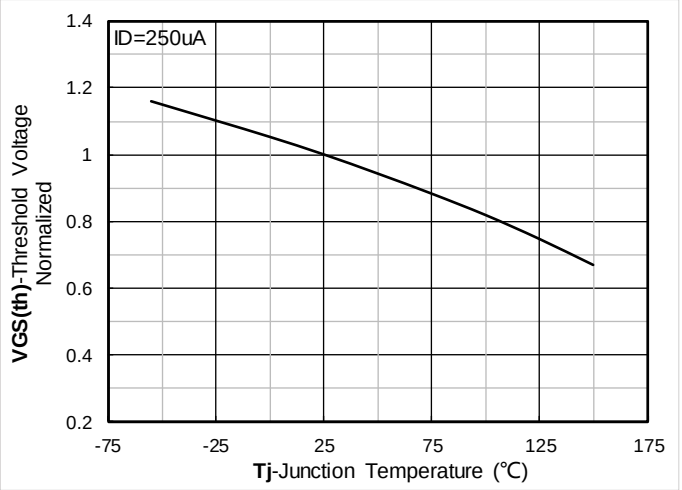



Figure 10. Normalized Threshold voltage

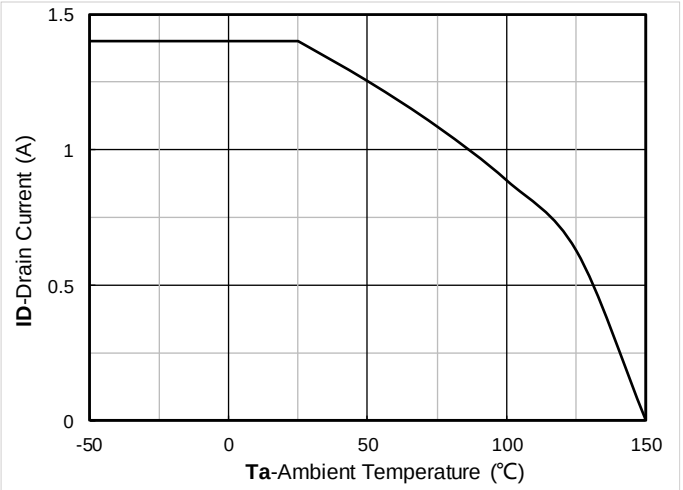



Figure 11. Current dissipation

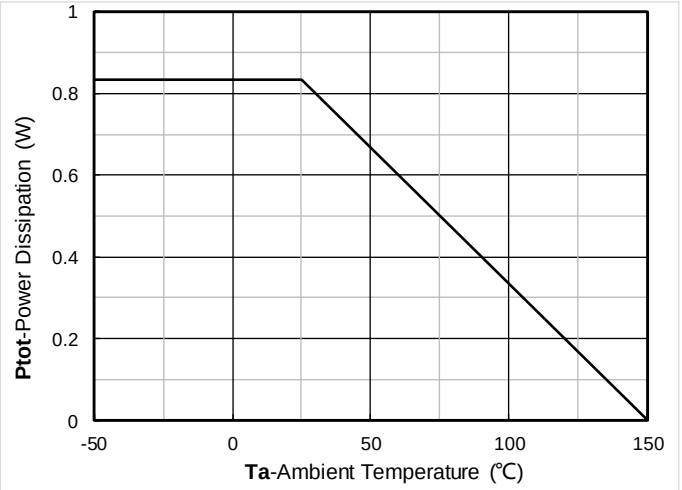



Figure 12. Power dissipation

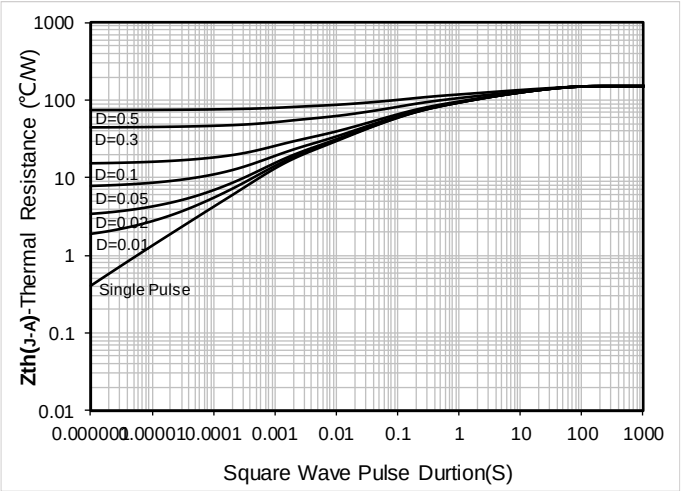



Figure 13. Maximum Transient Thermal Impedance

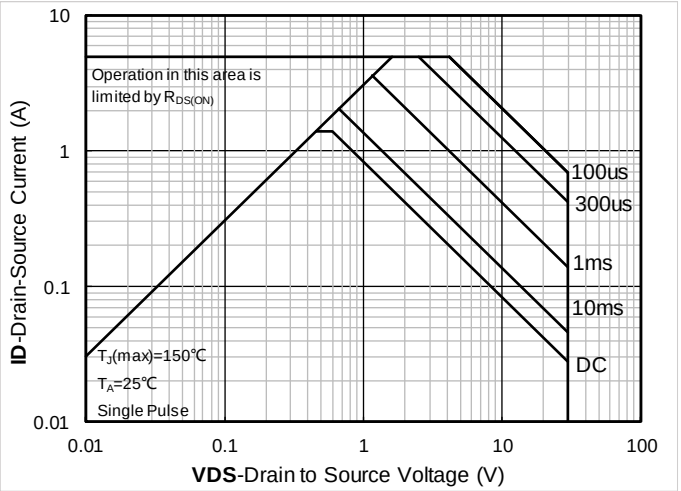
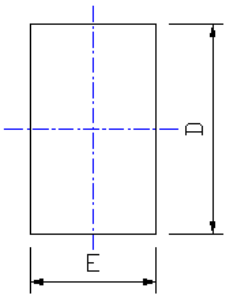
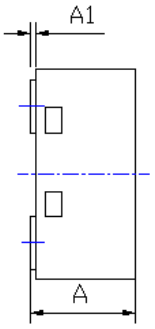



Figure 14. Safe Operation Area

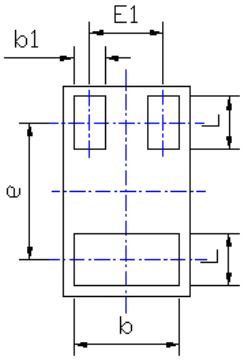
## ■ DFN1006-3L Package information



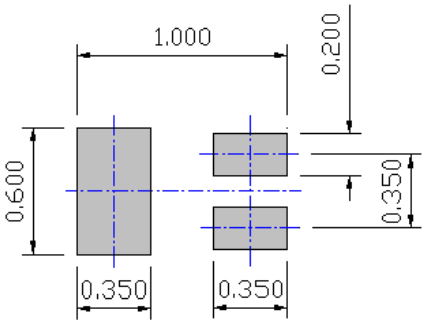

TOP VIEW




SIDE VIEW




BOTTOM VIEW




UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

| DIMENSIONS | | | |
|---|---|---|---|
| SYMBOL | Millimeter | | |
| | MIN. | NOM. | MAX. |
| A | 0.42 | --- | 0.55 |
| A1 | 0.025REF | | |
| b | 0.45 | 0.50 | 0.55 |
| b1 | 0.10 | 0.15 | 0.20 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.55 | 0.60 | 0.65 |
| E1 | 0.35BSC | | |
| e | 0.65BSC | | |
| L | 0.20 | 0.25 | 0.30 |

**NOTE:**
**1.PACKAGE BODY SIZES EXCLUDE LEAD BURRS.**
**2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.**
**3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.**

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