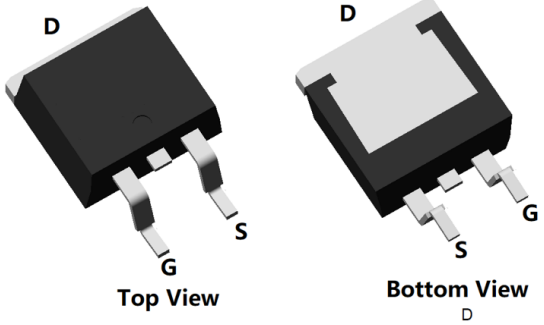
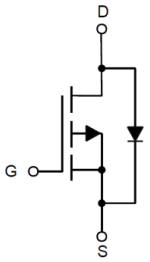
P-Channel Enhancement Mode Field Effect Transistor



TO-263



Product Summary

- V_{DS} -150V
- I_D -13A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜160mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜196mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power management
- Portable equipment
- Load switch

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	-150	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=-10V	I_D	-	-2.9	A
		T_A=100℃,V_{GS}=-10V		-	-1.8	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=-10V,Chip limitation		-	-13	
		T_C=100℃,V_{GS}=-10V		-	-8.2	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	-50	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		-13	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=-10V,R_G=25Ω,L=0.5mH,I_{AS}=-16.1A		EAS	-	64.8	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	2.8	W
		T_A=100℃		-	1.1	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	57.6	
		T_C=100℃		-	23	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	150	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	44	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	2.17	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
B160GP15A	F2	B160GP15A	800	1600	8000	13“ reel

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA,Tj=25℃	-150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-150V,V_{GS}=0V,Tj=25℃	-	-	-1	μA
		V_{DS}=-150V,V_{GS}=0V,Tj=150℃	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA,Tj=25℃	-1.4	-1.9	-2.4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V,I_D=-10A,Tj=25℃	-	121	160	mΩ
		V_{GS}=-4.5V,I_D=-5A,Tj=25℃	-	131	196	mΩ
Diode Forward Voltage	V_{SD}	I_S=-10A,V_{GS}=0V,Tj=25℃	-	-0.88	-1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	5	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-20V,V_{GS}=0V,f=1MHz,Tj=25℃	-	830	-	pF
Output Capacitance	C_{oss}		-	83	-	
Reverse Transfer Capacitance	C_{rss}		-	6.1	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-75V,I_D=-10A,Tj=25℃	-	17	-	nC
Gate-Source Charge	Q_{gs}		-	2.4	-	
Gate-Drain Charge	Q_{gd}		-	2.8	-	
Reverse Recovery Charge	Q_{rr}	I_F=-10A,di/dt=100A/μs,V_{GS}=0V, V_R=-75V,Tj=25℃	-	193	-	nC
Reverse Recovery Time	t_{rr}		-	66	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DS}=-75V,I_D=-10A,R_{GEN}=3Ω, Tj=25℃	-	5.4	-	ns
Turn-on Rise Time	t_r		-	4	-	
Turn-off Delay Time	$t_{D(off)}$		-	22	-	
Turn-off Fall Time	t_f		-	7.4	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

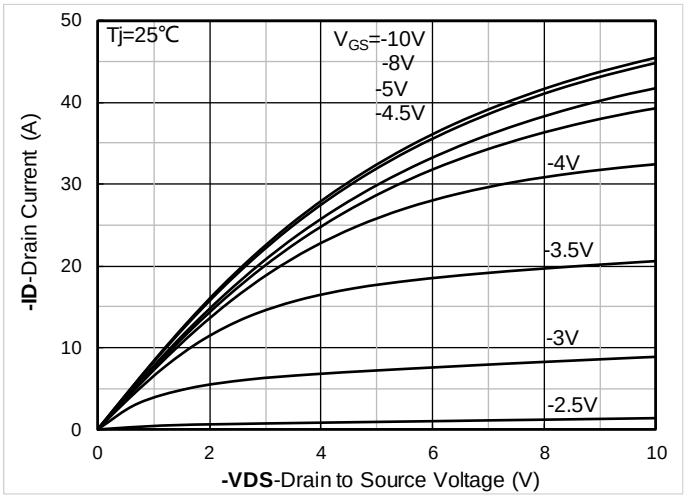


Figure 1. Output Characteristics; typical values

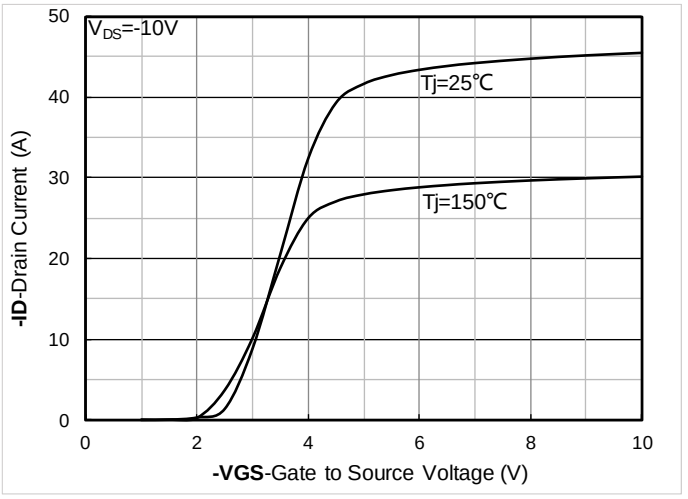


Figure 2. Transfer Characteristics; typical values

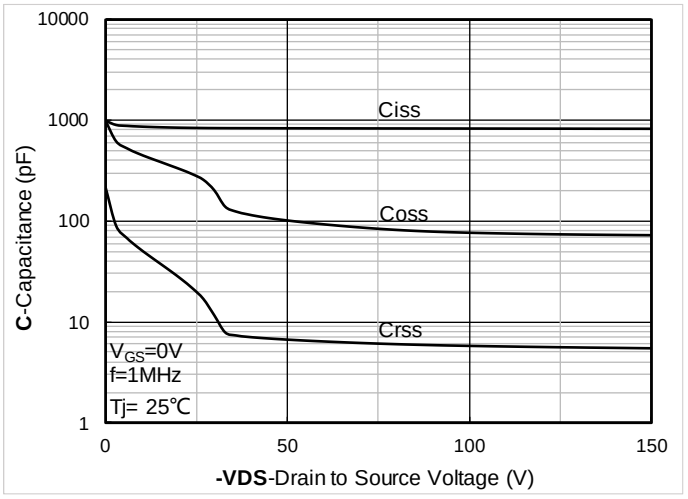


Figure 3. Capacitance Characteristics; typical values

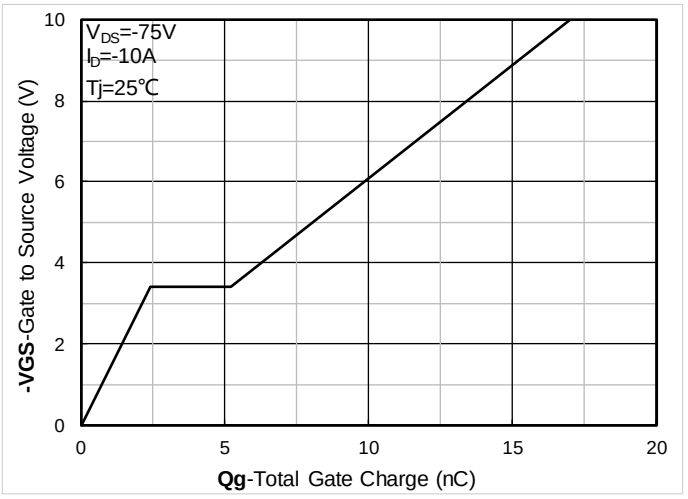


Figure 4. Gate Charge; typical values

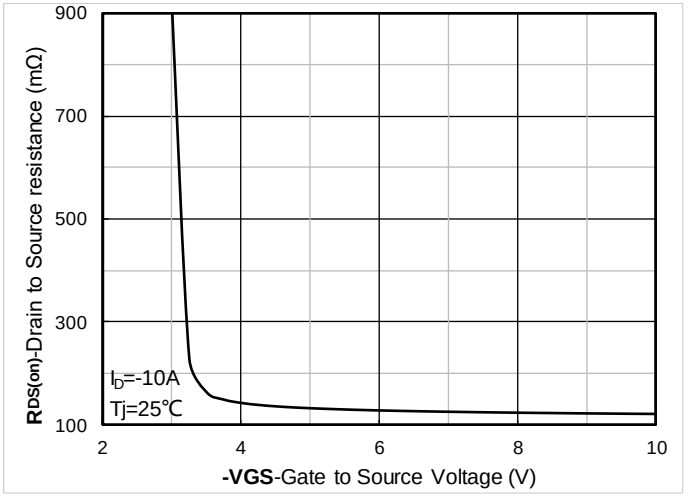


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

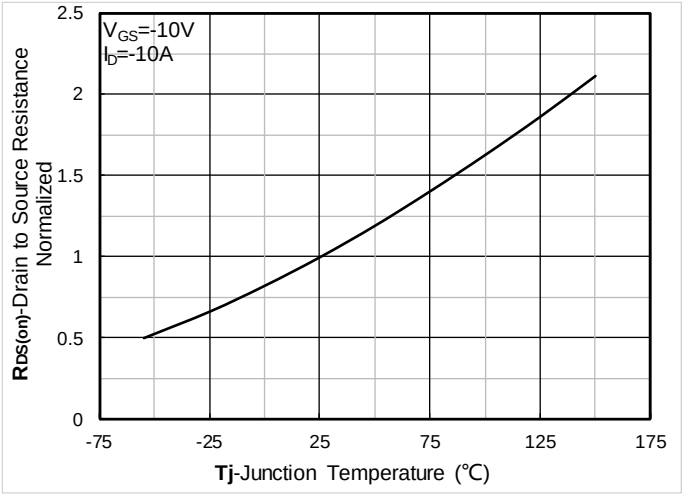


Figure 6. Normalized On-Resistance

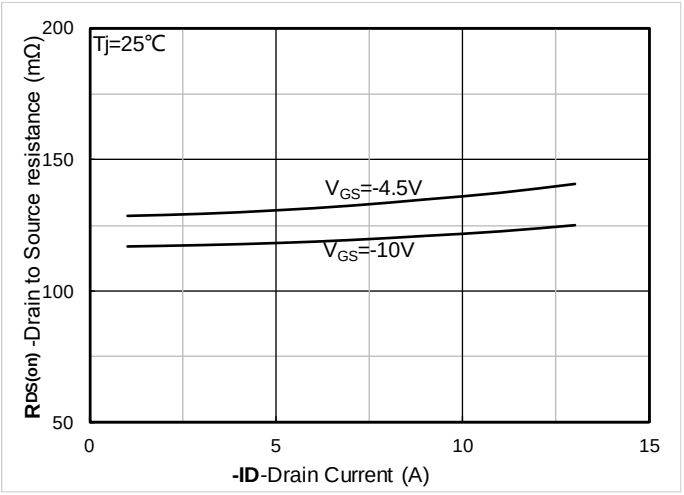


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

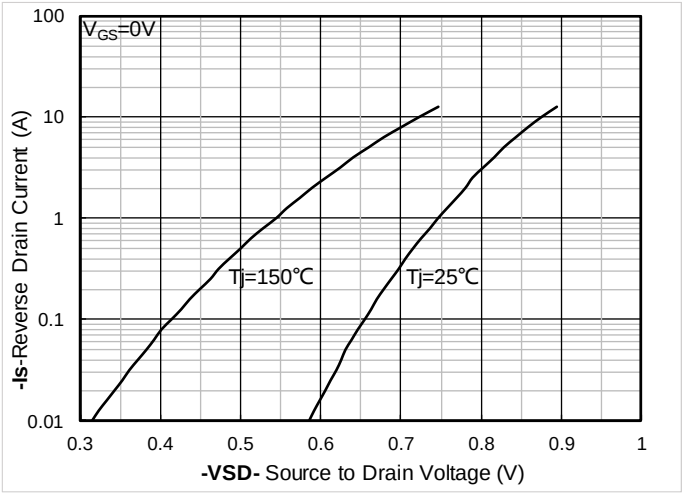


Figure 8. Forward characteristics of reverse diode; typical values

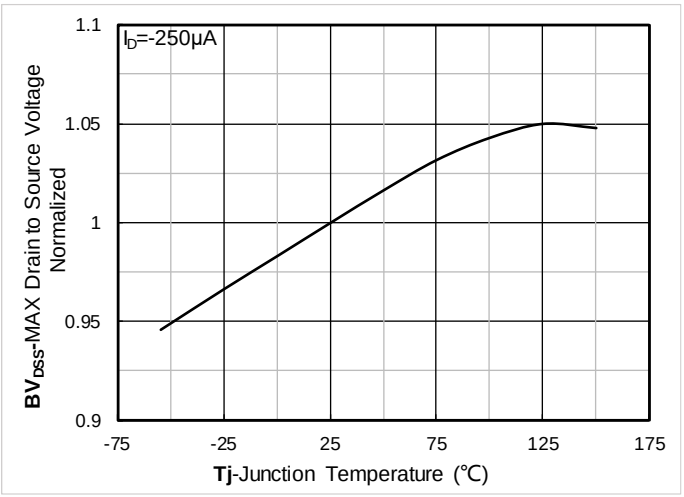


Figure 9. Normalized breakdown voltage

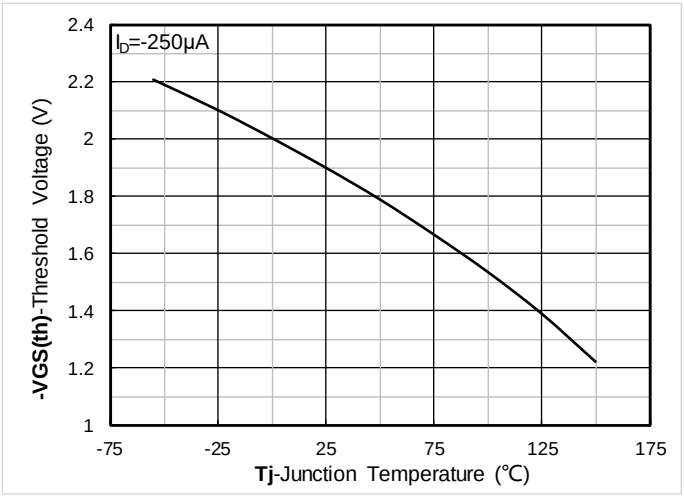


Figure 10. Gate Threshold voltage; typical values

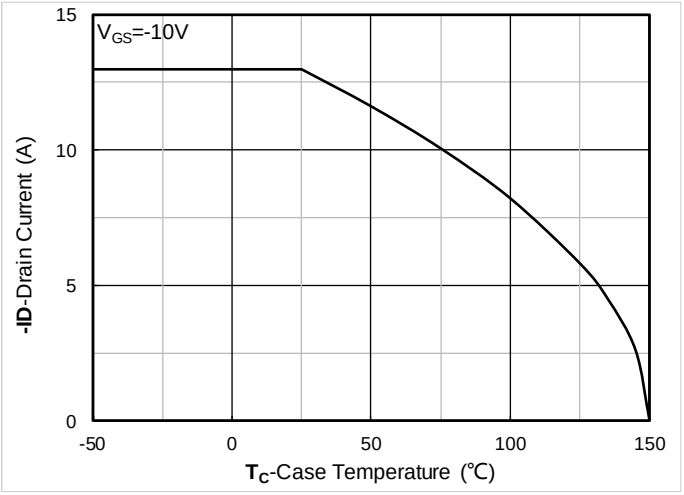


Figure 11. Current dissipation

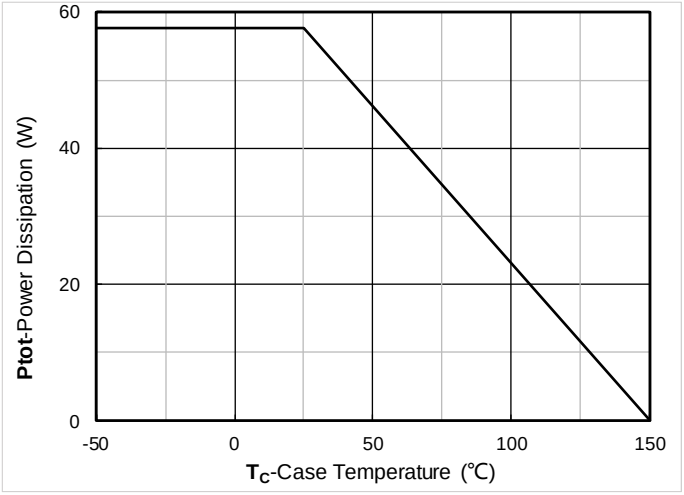


Figure 12. Power dissipation

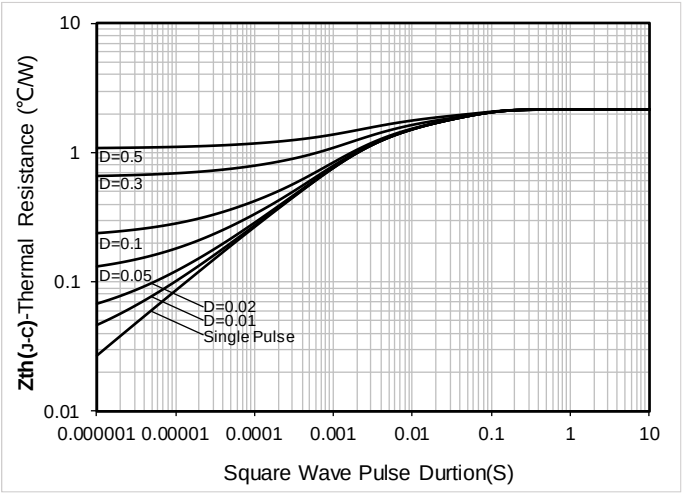


Figure 13. Maximum Transient Thermal Impedance

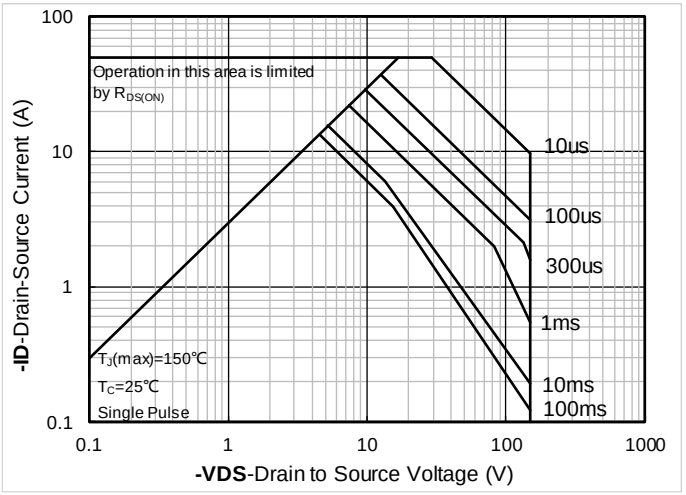
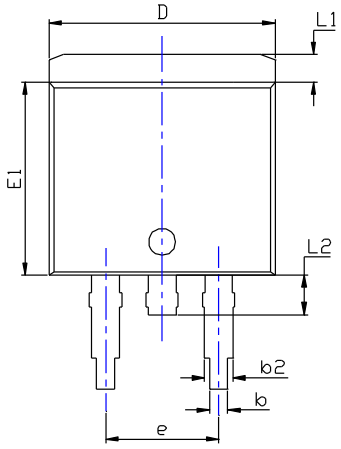
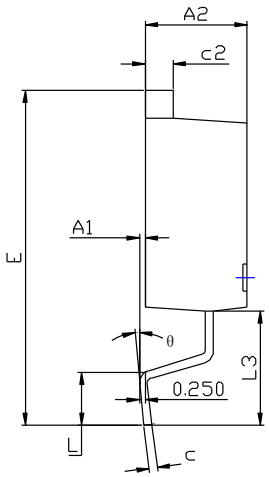


Figure 14. Safe Operation Area

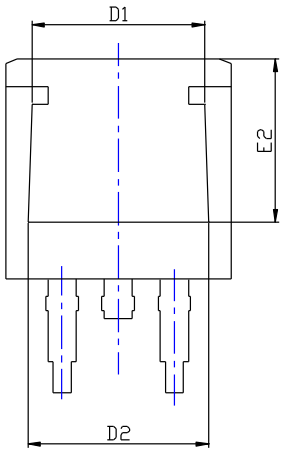
■ TO-263-HY Package information



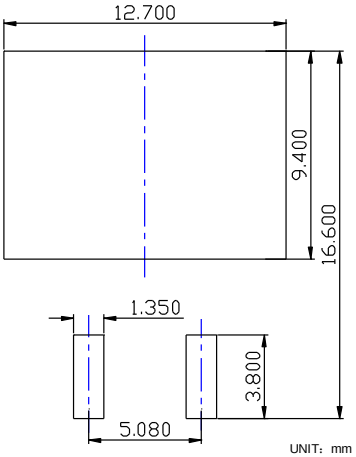
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
θ	0°	---	8°	0°	---	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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