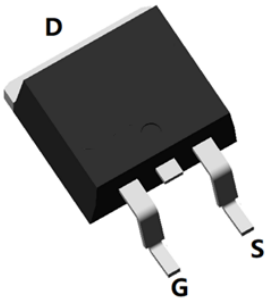
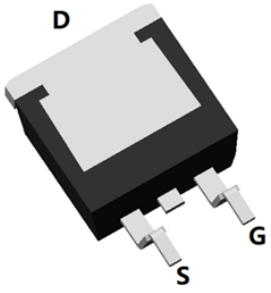
N-Channel Enhancement Mode Field Effect Transistor

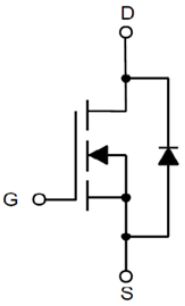


Top View



Bottom View

TO-263



Product Summary

- V_{DS} 100V
- I_D 140A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜3.9mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Wide safe operating area
- Moisture Sensitivity Level 1
- Halogen Free
- Epoxy Meets UL 94 V-0 Flammability Rating
- Wide safe operating area SOA

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- Hot Swap Application

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	100	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	17	A
		T_A=100℃,V_{GS}=10V		-	12	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V,Chip limitation		-	140	
		T_C=100℃,V_{GS}=10V		-	99	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	560	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		140	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=10V,R_G=25Ω,L=0.5mH,I_{AS}=45A		EAS	-	506	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	3.7	W
		T_A=100℃		-	1.8	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	246	
		T_C=100℃		-	123	
I_{Pulse}	T_C=25℃,V_{DS}=50V,t_p=10ms		I_{SOA}	-	2.68	A
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	175	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	40	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.61	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
B3D9G10HJS	F2	B3D9G10HJS	800	/	4000	13“ reel

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=1mA,Tj=25℃	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=100V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2.2	3	3.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=30A,Tj=25℃	-	3	3.9	mΩ
Diode Forward Voltage	V_{SD}	I_S=30A,V_{GS}=0V,Tj=25℃	-	0.83	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	2.1	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=0.5MHz,Tj=25℃	-	4673	-	pF
Output Capacitance	C_{oss}		-	1785	-	
Reverse Transfer Capacitance	C_{rss}		-	18	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=70A,Tj=25℃	-	63.7	-	nC
Gate-Source Charge	Q_{gs}		-	25	-	
Gate-Drain Charge	Q_{gd}		-	12.4	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs,V_{GS}=0V,V_R=50V,Tj=25℃	-	68	-	nC
Reverse Recovery Time	t_{rr}		-	54	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=50V,I_D=70A,R_{GEN}=1Ω, Tj=25℃	-	18	-	ns
Turn-on Rise Time	t_r		-	75	-	
Turn-off Delay Time	$t_{D(off)}$		-	33	-	
Turn-off Fall Time	t_f		-	18	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

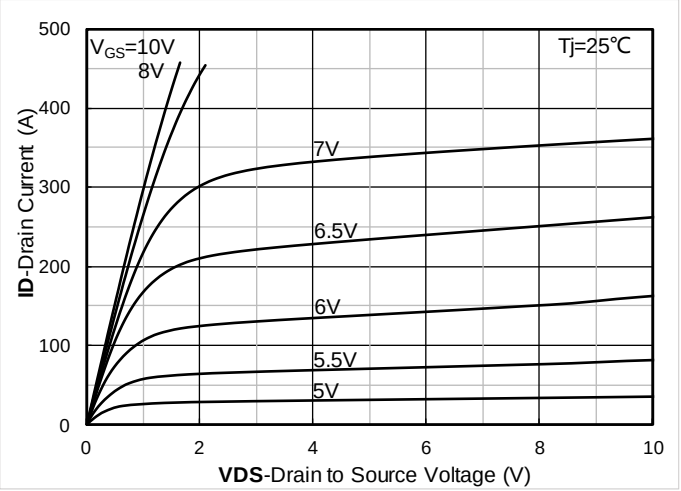


Figure 1. Output Characteristics; typical values

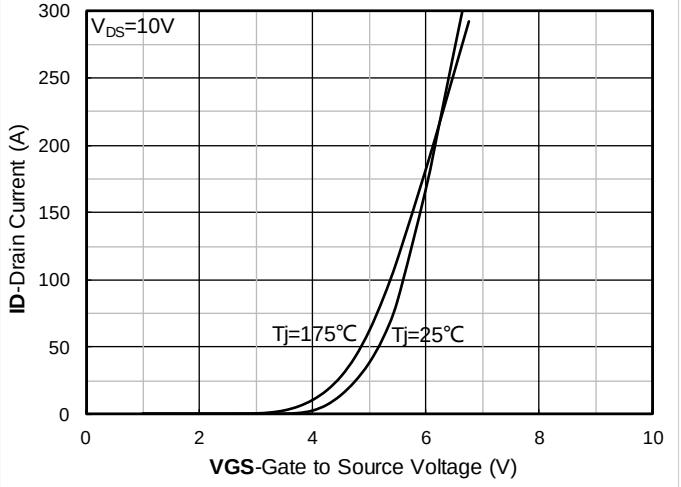


Figure 2. Transfer Characteristics; typical values

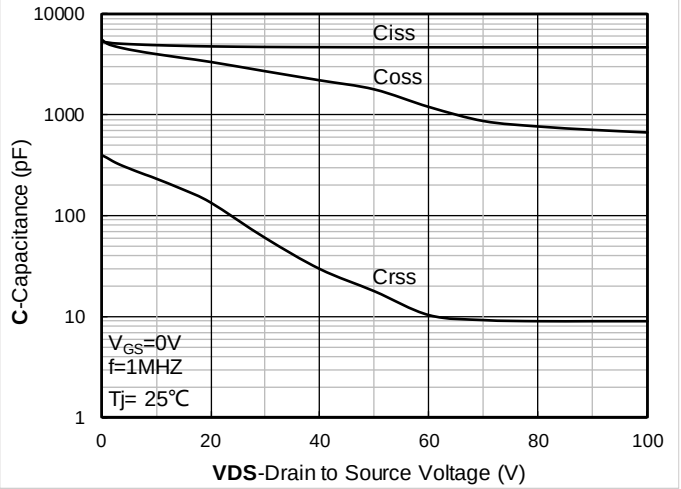


Figure 3. Capacitance Characteristics; typical values

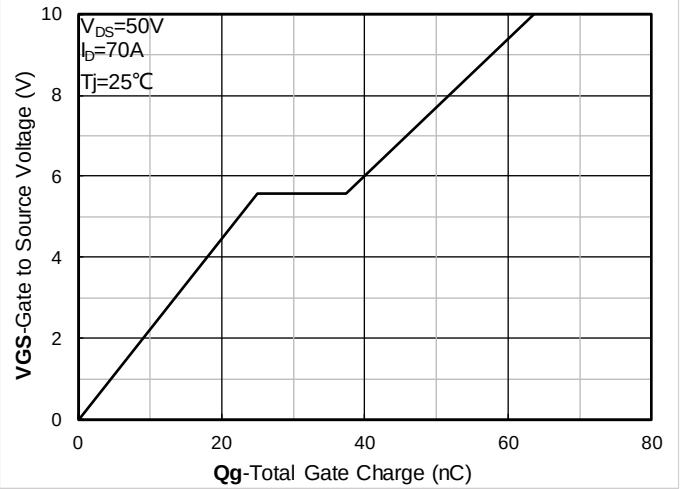


Figure 4. Gate Charge; typical values

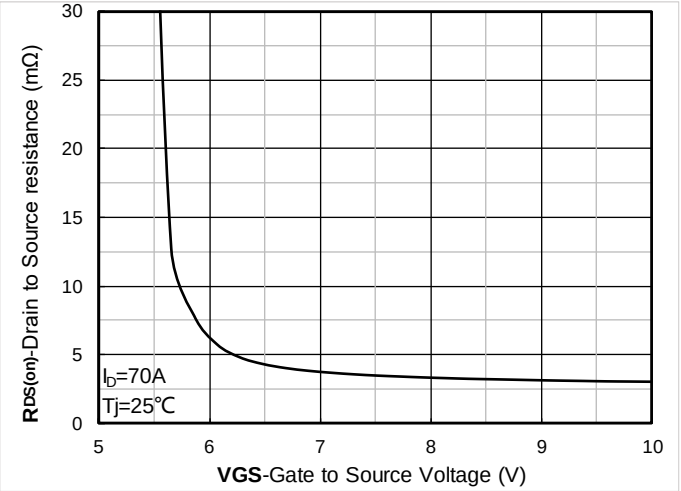


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

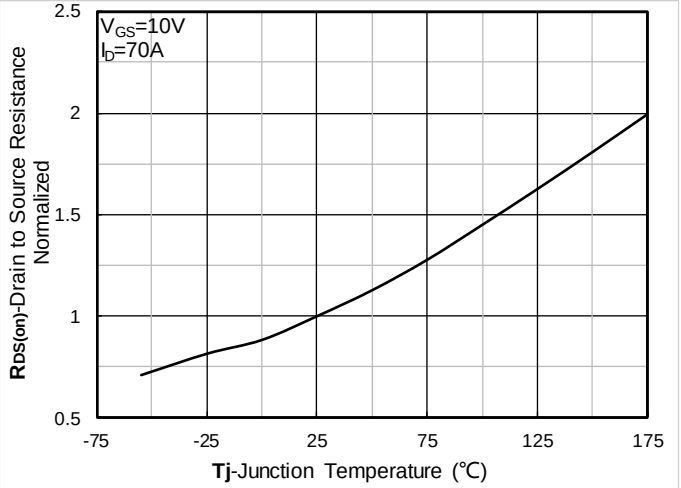


Figure 6. Normalized On-Resistance

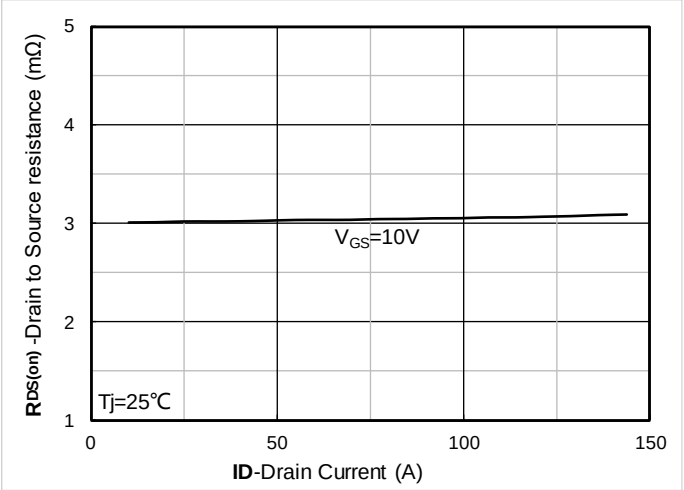


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

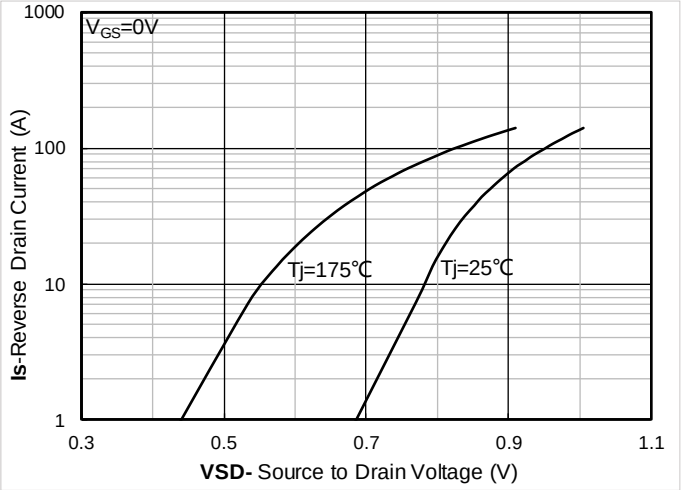


Figure 8. Forward characteristics of reverse diode; typical values

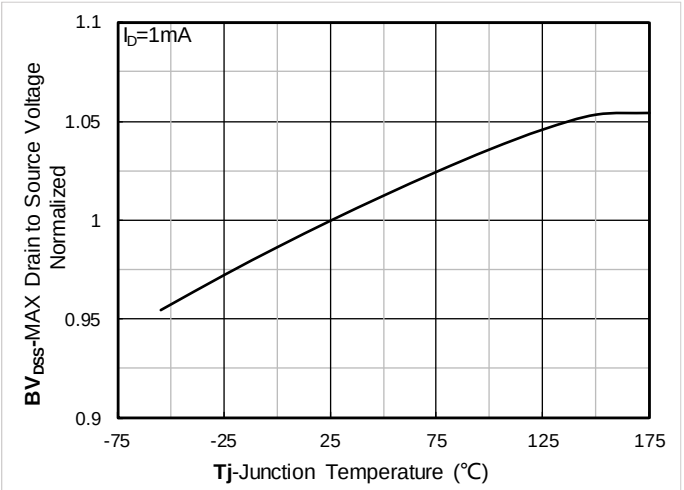


Figure 9. Normalized breakdown voltage

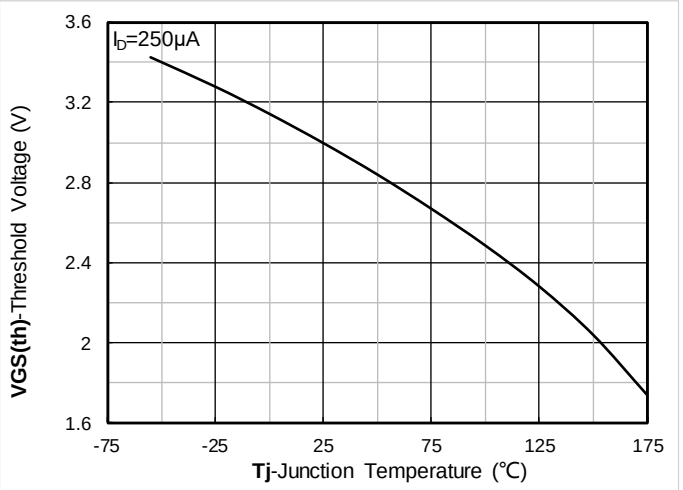


Figure 10. Gate Threshold voltage; typical values

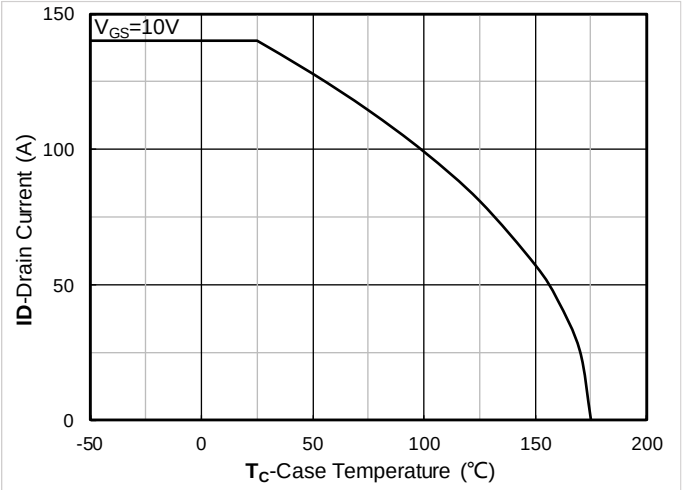


Figure 11. Current dissipation

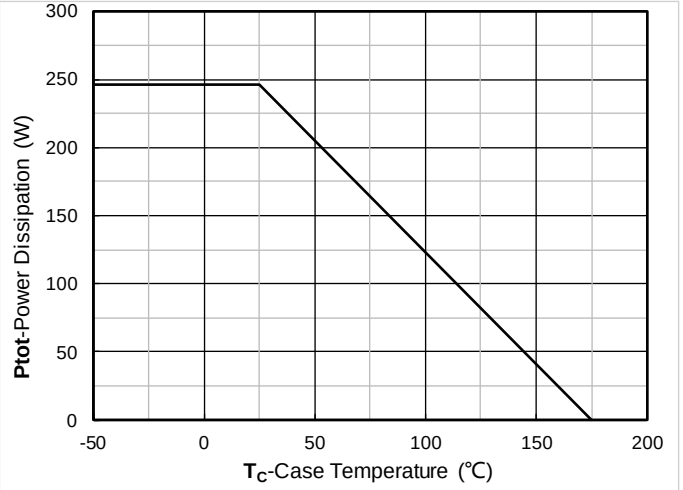


Figure 12. Power dissipation

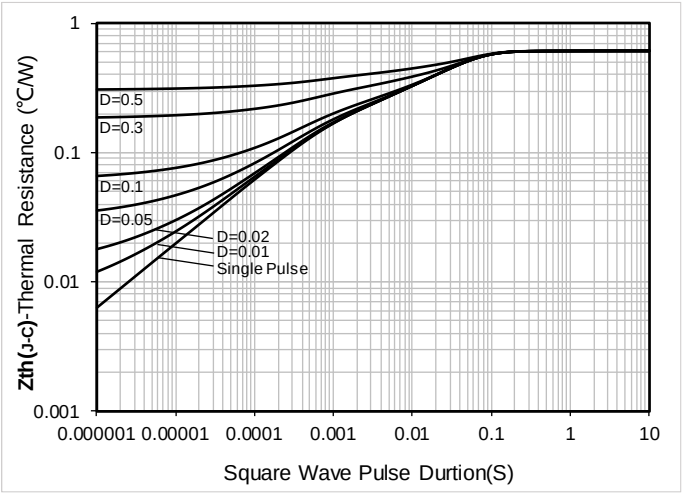


Figure 13. Maximum Transient Thermal Impedance

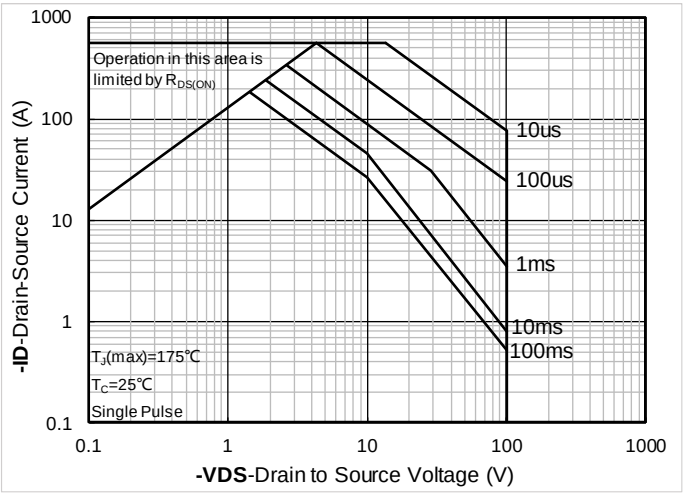
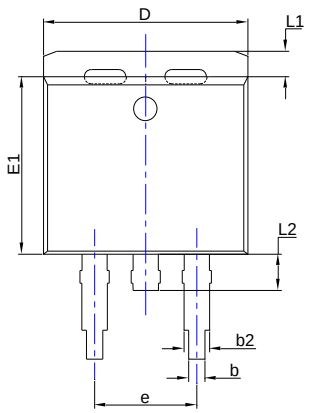
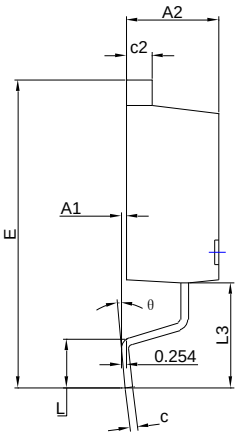


Figure 14. Safe Operation Area

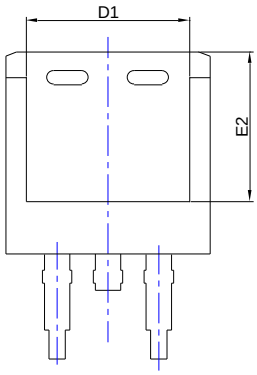
■ TO-263-B Package information



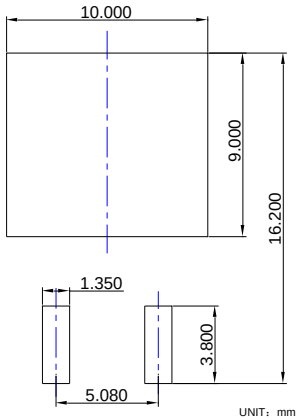
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		MILLIMETER	
	MIN.	MAX.	MIN.	MAX.
A1	0.000	0.010	0.000	0.254
A2	0.160	0.190	4.064	4.826
b	0.020	0.039	0.508	0.991
b2	0.045	0.070	1.143	1.778
c	0.015	0.029	0.381	0.737
c2	0.045	0.065	1.143	1.651
D	0.380	0.420	9.652	10.668
D1	0.245	---	6.223	---
E	0.575	0.625	14.605	15.875
E1	0.330	0.380	8.382	9.652
E2	0.270	---	6.858	---
e	0.200BSC		5.08BSC	
L	0.070	0.110	1.778	2.794
L1	---	0.066	---	1.676
L2	---	0.070	---	1.778
L3	0.188	0.208	4.780	5.280
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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