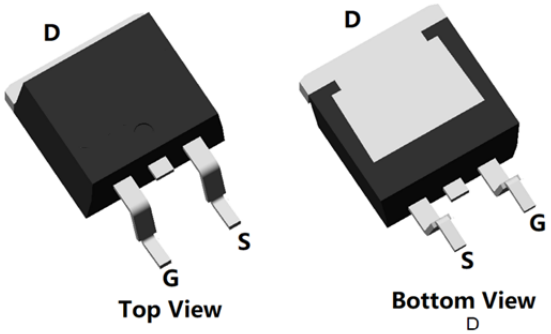
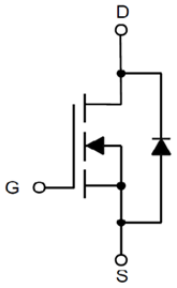
N-Channel Enhancement Mode Field Effect Transistor



TO-263



Product Summary

- V_{DS} 60V
- I_D 90A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜5.0mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings (T_J=25℃ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	60	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃	I_D	18.5	A
		T_A=100℃		13	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃		90	
		T_C =100℃		63	
Pulsed Drain Current	T_C=25℃, t_p=100μs		I_{DM}	350	A
Avalanche energy	V_G=10V, R_G=25Ω, L=0.5mH, IAS=23A		EAS	132.25	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	3.7	W
		T_A=100℃		1.8	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		93	
		T_C =100℃		46	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55～+175	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	33	40	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.3	1.6	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
B5D0G06H	F2	B5D0G06H	800	/	8000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V	-	-	1	μA
		V_{DS}=60V, V_{GS}=0V, Tj=125℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-	3.9	5.0	mΩ
Diode Forward Voltage	V_{SD}	I_S=40A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	1.5	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	90	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V, V_{GS}=0V, f=1MHz	-	1550	-	pF
Output Capacitance	C_{oss}		-	460	-	
Reverse Transfer Capacitance	C_{rss}		-	16	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=30V, I_D=37.5A	-	26	-	nC
Gate-Source Charge	Q_{gs}		-	6	-	
Gate-Drain Charge	Q_{gd}		-	14	-	
Reverse Recovery Charge	Q_{rr}	I_F=37.5A, di/dt=270A/us	-	37	-	nC
Reverse Recovery Time	t_{rr}		-	28	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=30V, I_D=37.5A R_{GEN}=2.2Ω	-	13	-	ns
Turn-on Rise Time	t_r		-	147	-	
Turn-off Delay Time	$t_{D(off)}$		-	19	-	
Turn-off fall Time	t_f		-	4	-	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

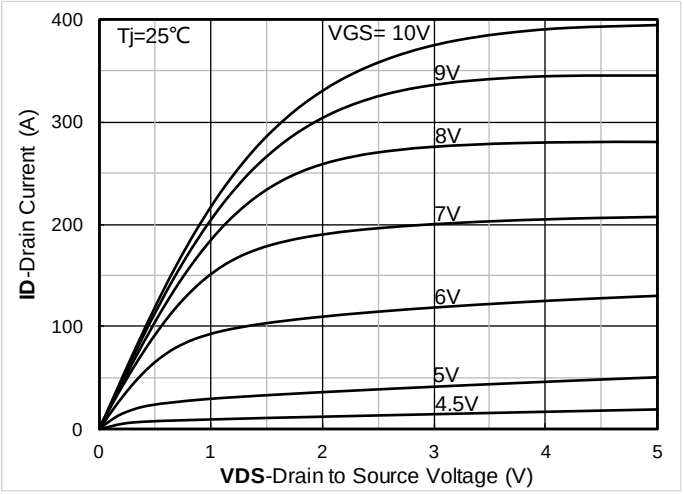


Figure 1. Output Characteristics

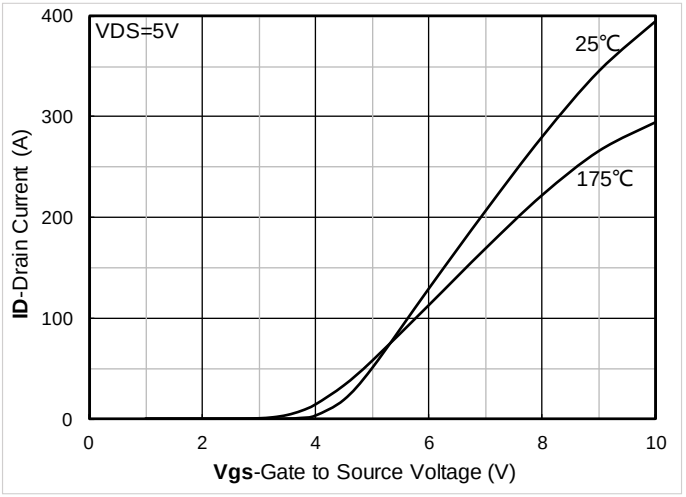


Figure 2. Transfer Characteristics

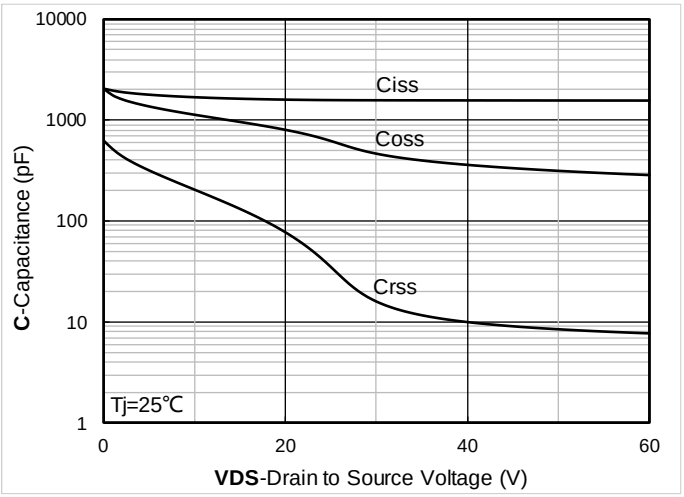


Figure 3. Capacitance Characteristics

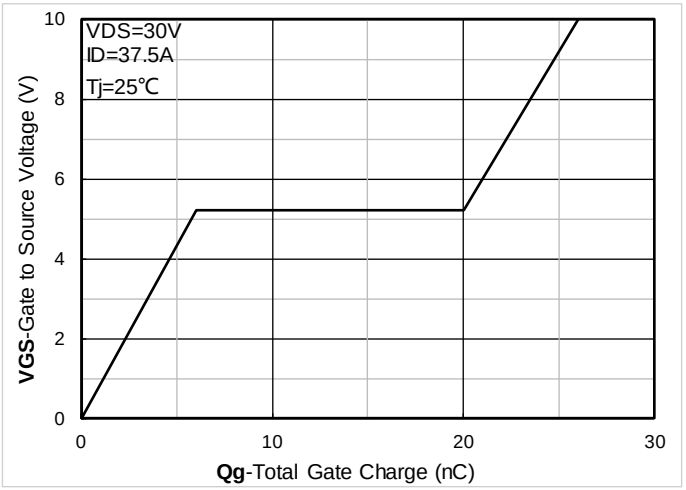


Figure 4. Gate Charge

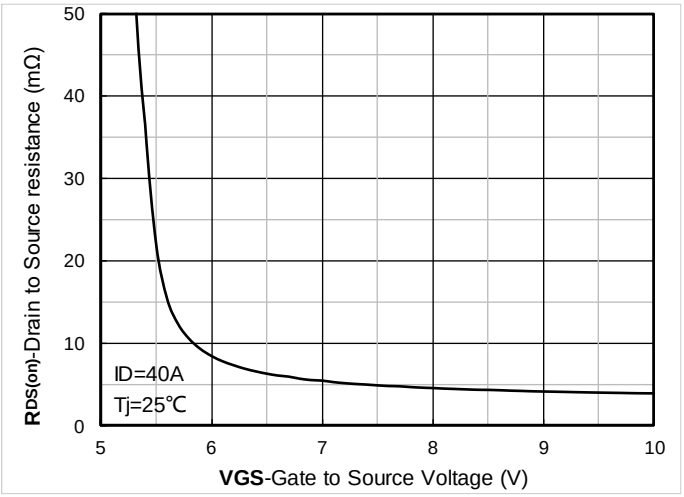


Figure 5. On-Resistance vs Gate to Source Voltage

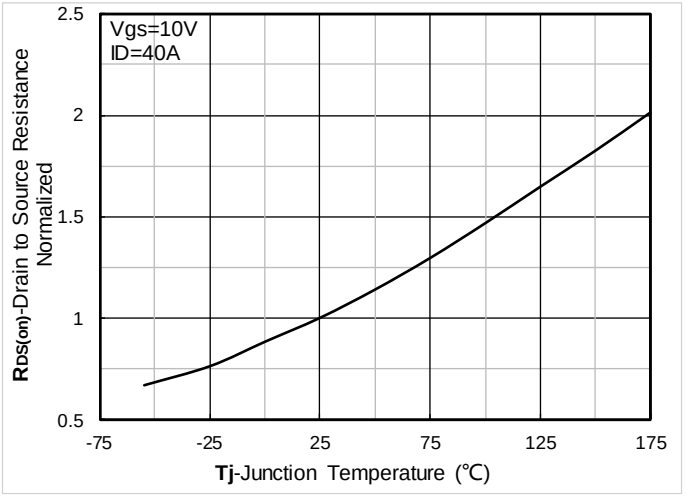


Figure 6. Normalized On-Resistance

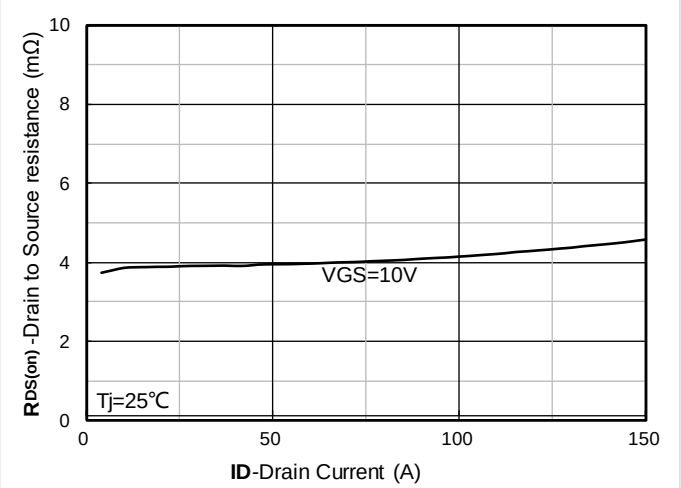


Figure 7. $R_{DS(on)}$ VS Drain Current

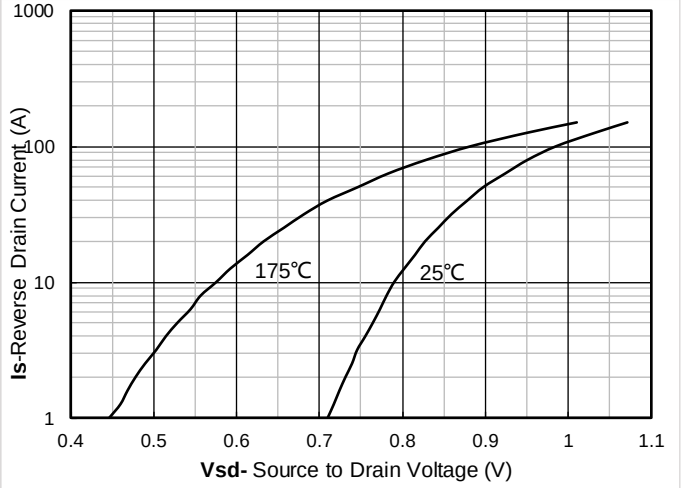


Figure 8. Forward characteristics of reverse diode

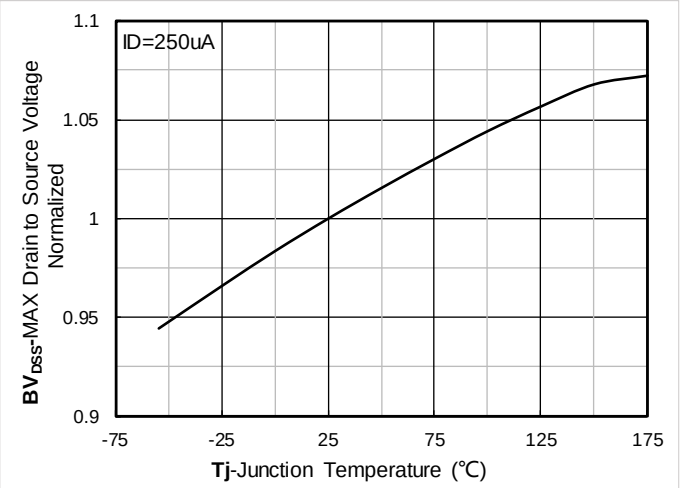


Figure 9. Normalized breakdown voltage

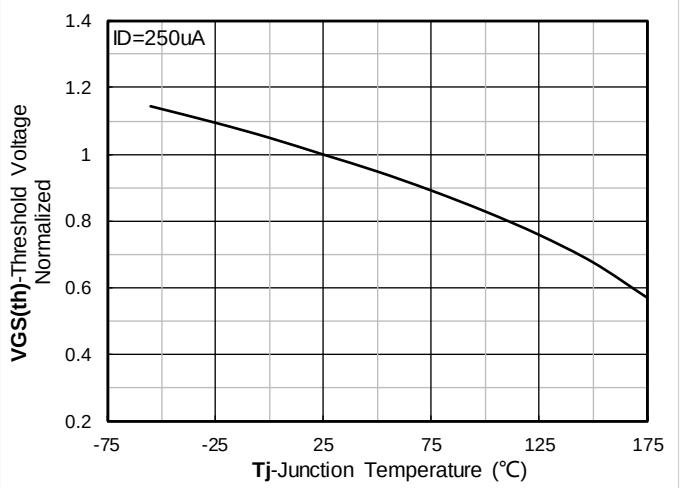


Figure 10. Normalized Threshold voltage

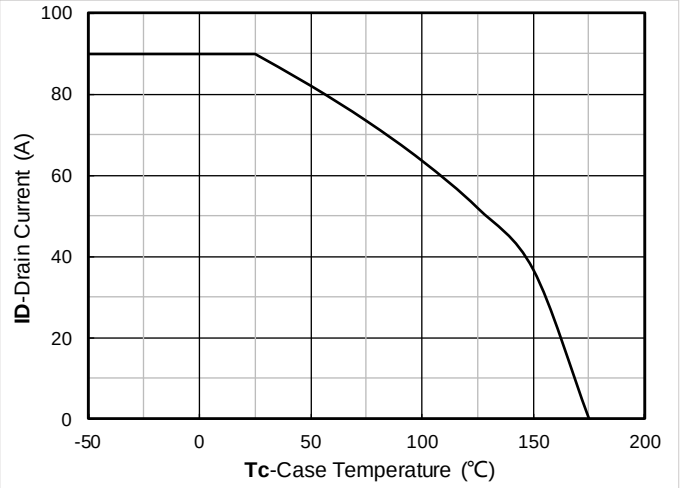


Figure 11. Current dissipation

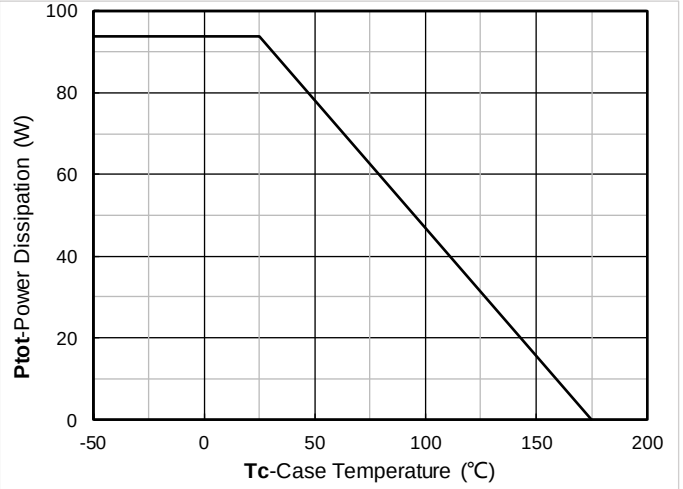


Figure 12. Power dissipation

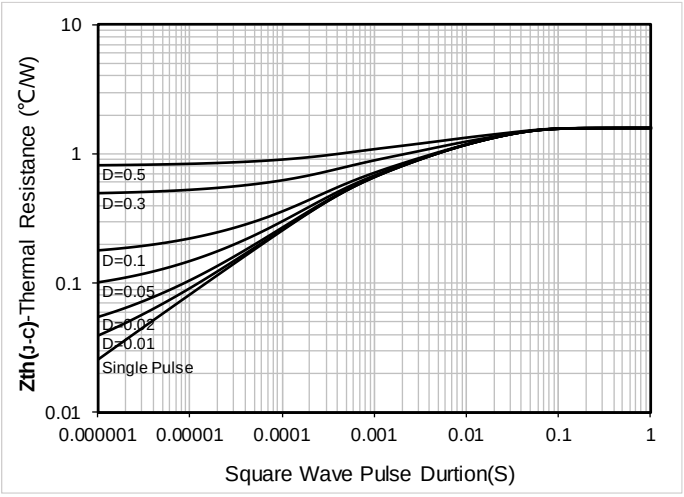


Figure 13. Maximum Transient Thermal Impedance

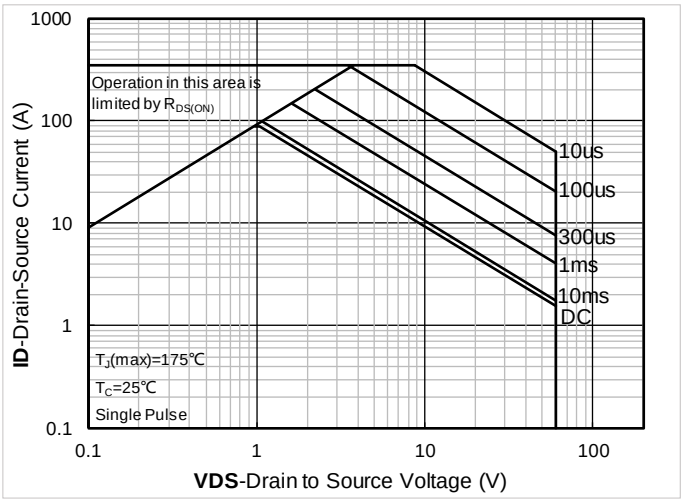
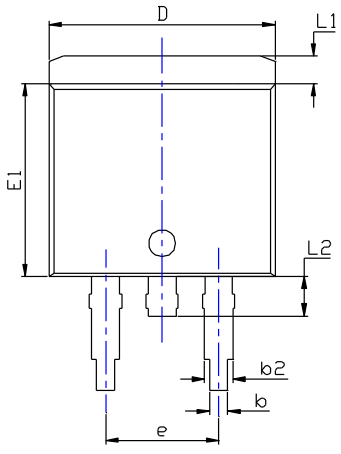
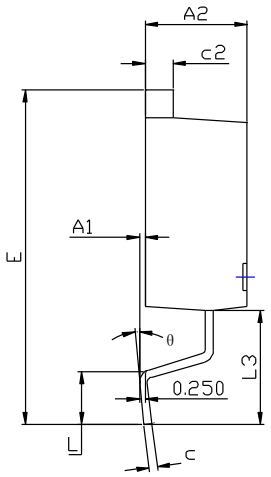


Figure 14. Safe Operation Area

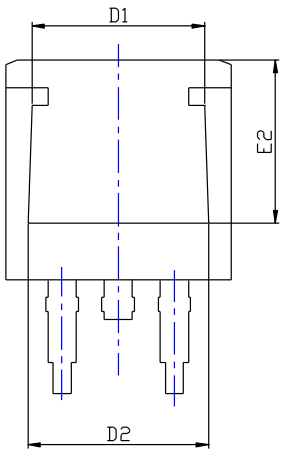
■ TO-263-HY Package information



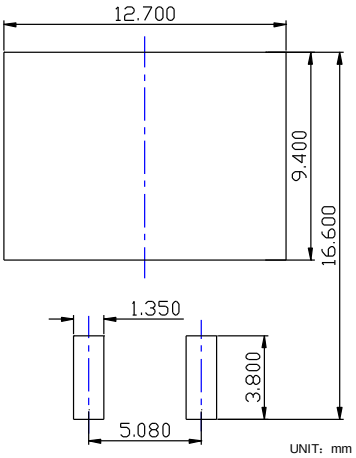
TOP VIEW



SIDE VIEW



BOTTOM VIEW



SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.280	1.340
D	0.394	0.400	0.406	10.000	10.150	10.300
D1	0.295	0.307	0.319	7.500	7.800	8.100
D2	0.303	0.315	0.327	7.700	8.000	8.300
E	0.571	0.591	0.610	14.500	15.000	15.500
E1	0.337	0.341	0.348	8.550	8.700	8.850
E2	0.276	0.287	0.299	7.000	7.300	7.600
e	0.200BSC			5.080BSC		
L	0.070	---	0.110	1.790	---	2.790
L1	0.044	---	0.056	1.120	---	1.420
L2	0.030	---	0.070	0.770	---	1.770
L3	0.197REF			5.000REF		
θ	0°	---	8°	0°	---	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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