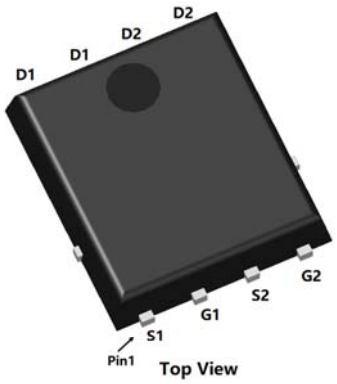
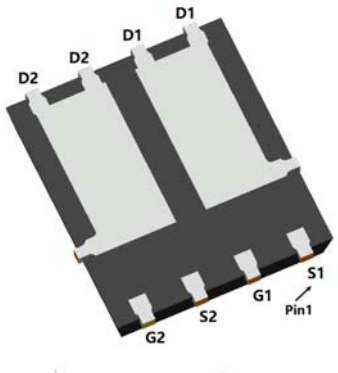
N-Channel and P-Channel Complementary MOSFET

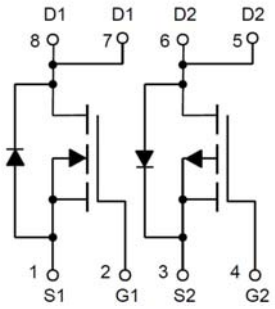


Top View



Bottom View

PDFN5060-8L



Product Summary

NMOS

- V_{DS} 100V
- I_D 40A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜19mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜23mΩ

PMOS

- V_{DS} -100V
- I_D -12A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜109mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜120mΩ

- 100% EAS Tested

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		V_{DS}	100	-100	V
Gate-source Voltage		V_{GS}	±20	±20	V
Drain Current	T_A=25℃	I_D	6.8	-2.8	A
	T_A=100℃		4.3	-1.8	
	T_C=25℃		40	-12	
	T_C =100℃		25	-7.6	
Pulsed Drain Current [A]		I_{DM}	120	-40	A
Avalanche energy [B]		EAS	72	64	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2	2	W
	T_A=100℃		0.8	0.8	
	T_C=25℃		69	44	
	T_C =100℃		27	17	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	-55～+150	℃

■Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	50	60	50	60	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.5	1.8	2.3	2.8	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
G12NP10B	F1	G12NP10B	5000	10000	100000	13“ reel

■ NMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.2	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	15	19	mΩ
		V_{GS}=4.5V, I_D=5A	-	18	23	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	1.5	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	40	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	1150	-	pF
Output Capacitance	C_{oss}		-	430	-	
Reverse Transfer Capacitance	C_{rss}		-	8	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=20A	-	20	-	nC
Gate-Source Charge	Q_{gs}		-	5.6	-	
Gate-Drain Charge	Q_{gd}		-	2.8	-	
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=100A/us	-	32	-	nC
Reverse Recovery Time	t_{rr}		-	41	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V, I_D=20A R_{GEN}=3Ω	-	7	-	ns
Turn-on Rise Time	t_r		-	29	-	
Turn-off Delay Time	$t_{D(off)}$		-	18	-	
Turn-off fall Time	t_f		-	7	-	

■ PMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V	-	-	-1	μA
		V_{DS}=-100V, V_{GS}=0V, Tj=150℃	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-12A	-	84	109	mΩ
		V_{GS}=-4.5V, I_D=-3A	-	89	120	
Diode Forward Voltage	V_{SD}	I_S=-12A, V_{GS}=0V	-	-	-1.2	V
Gate resistance	R_G	f=1MHz	-	10	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-12	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-50V, V_{GS}=0V, f=1MHz	-	1060	-	pF
Output Capacitance	C_{oss}		-	110	-	
Reverse Transfer Capacitance	C_{rss}		-	8	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-50V, I_D=-10A	-	19.5	-	nC
Gate-Source Charge	Q_{gs}		-	4.4	-	
Gate-Drain Charge	Q_{gd}		-	3.7	-	
Reverse Recovery Charge	Q_{rr}	I_F=-10A, di/dt=100A/us	-	90	-	nC
Reverse Recovery Time	t_{rr}		-	59	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DD}=-50V, ID=-10A R_{GEN}=3Ω	-	7.4	-	ns
Turn-on Rise Time	t_r		-	31	-	
Turn-off Delay Time	$t_{D(off)}$		-	48	-	
Turn-off fall Time	t_f		-	65	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. NMOS: T_J=25℃, V_G=10V, R_G=25Ω, L=0.5mH, IAS=17A.
PMOS: T_J=25℃, V_G=-10V, R_G=25Ω, L=0.5mH, IAS=-16A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

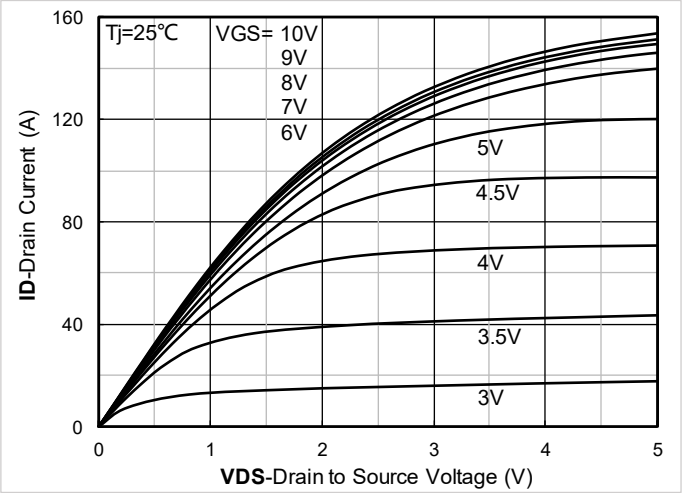


Figure 1. Output Characteristics

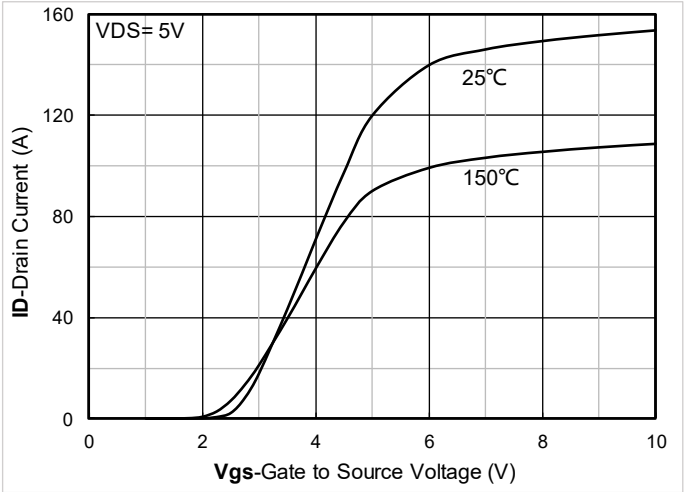


Figure 2. Transfer Characteristics

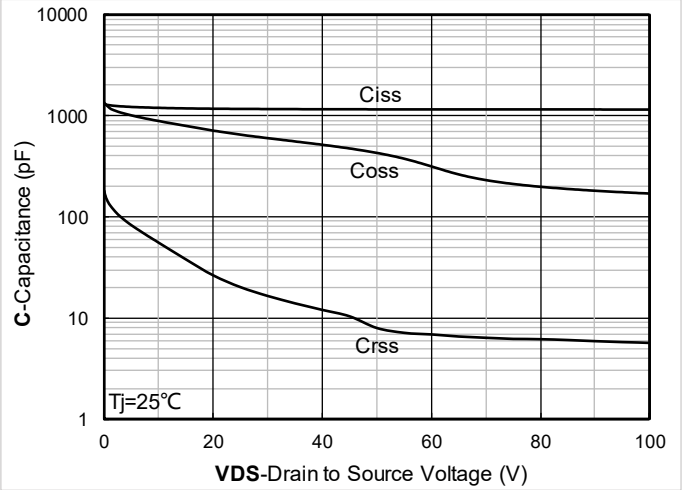


Figure 3. Capacitance Characteristics

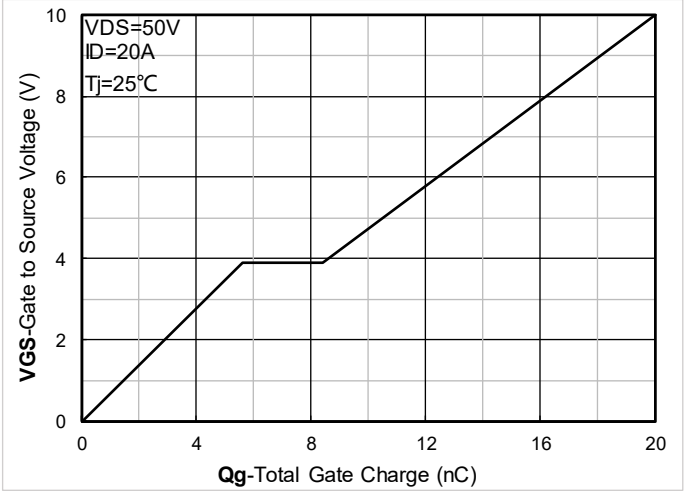


Figure 4. Gate Charge

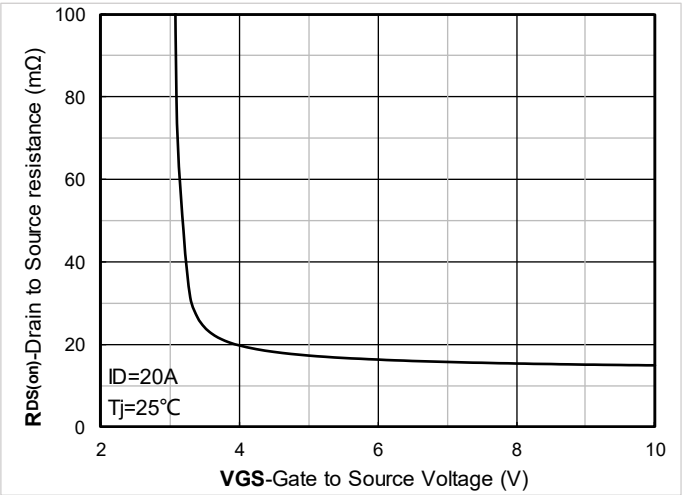


Figure 5. On-Resistance vs Gate to Source Voltage

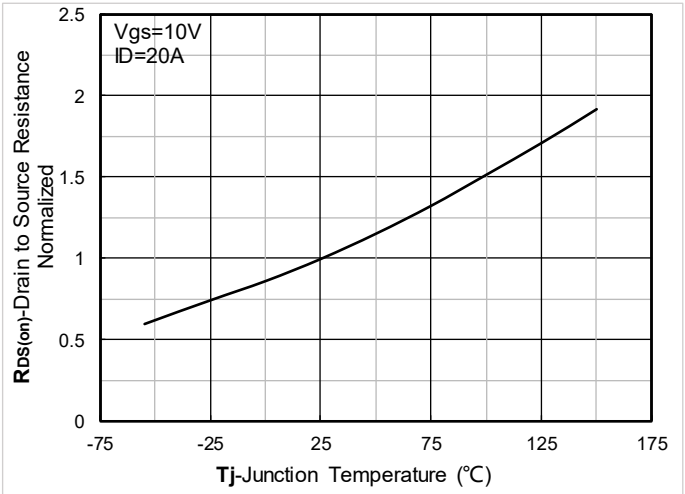


Figure 6. Normalized On-Resistan

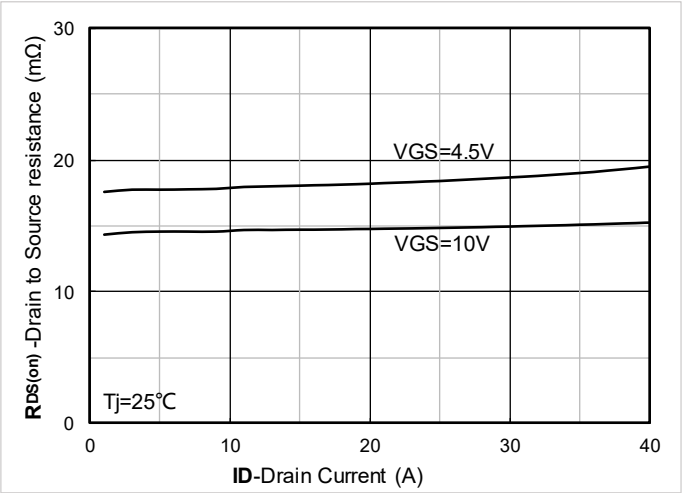


Figure 7. $R_{DS(on)}$ VS Drain Current

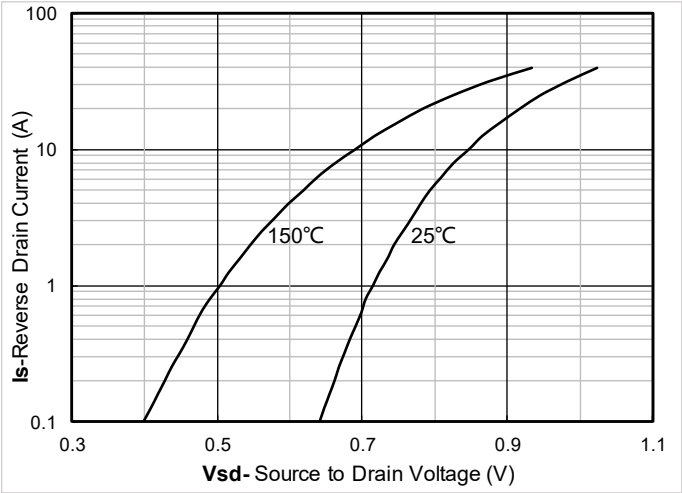


Figure 8. Forward characteristics of reverse diode

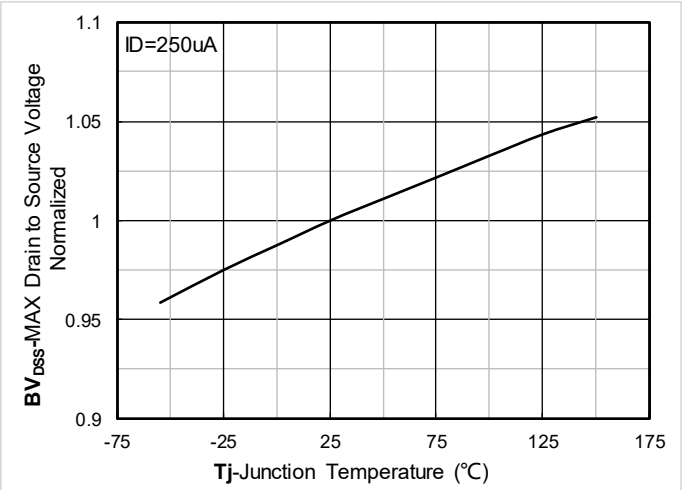


Figure 9. Normalized breakdown voltage

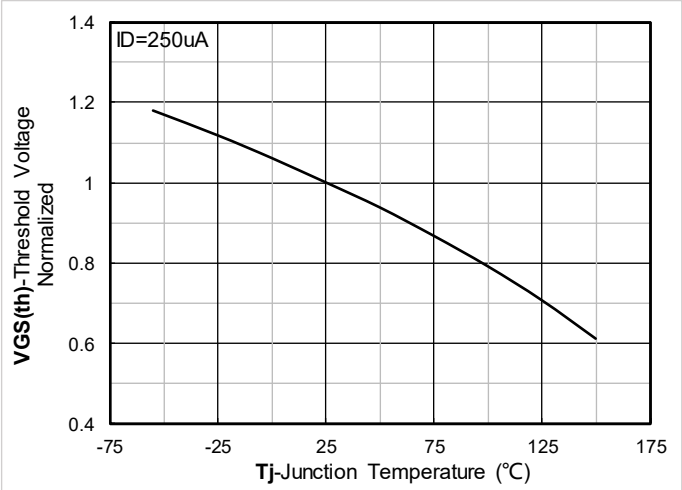


Figure 10. Normalized Threshold voltage

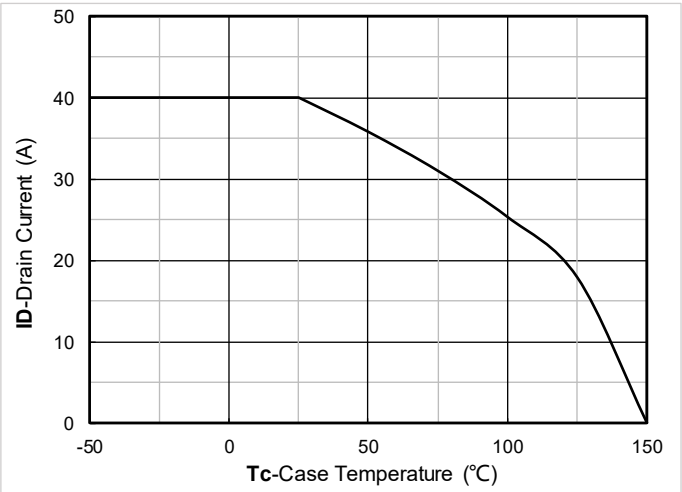


Figure 11. Current dissipation

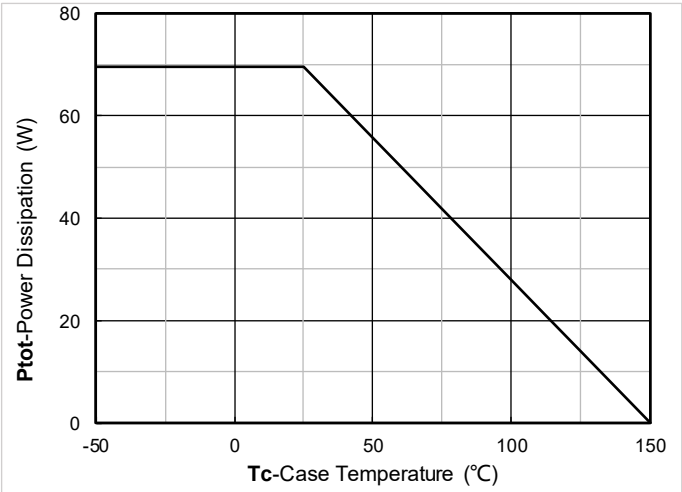


Figure 12. Power dissipation

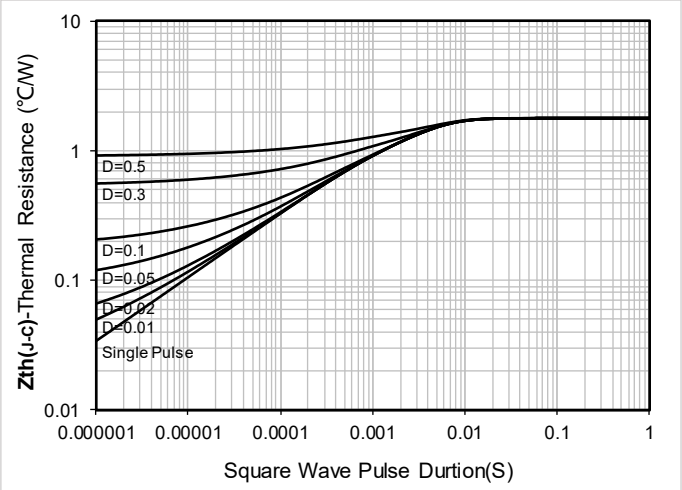


Figure 13. Maximum Transient Thermal Impedance

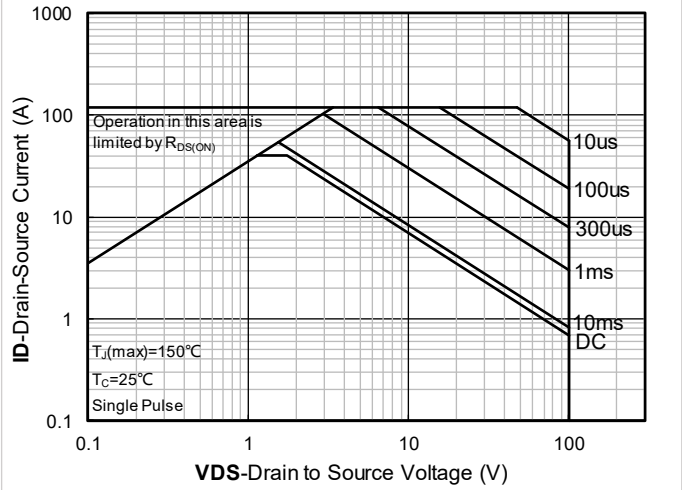


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

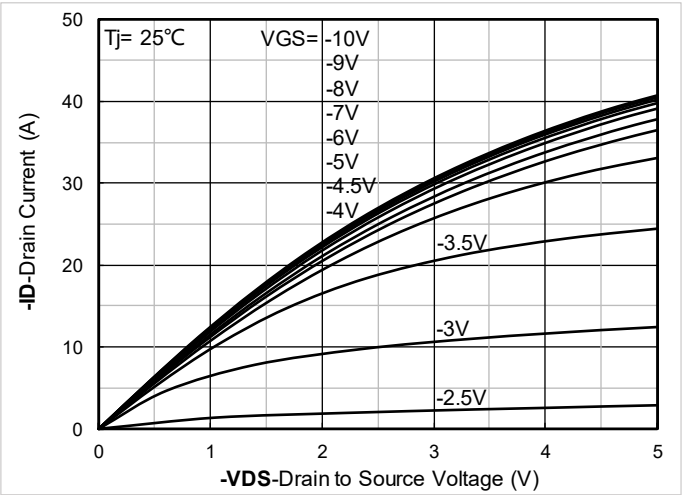


Figure 1. Output Characteristics

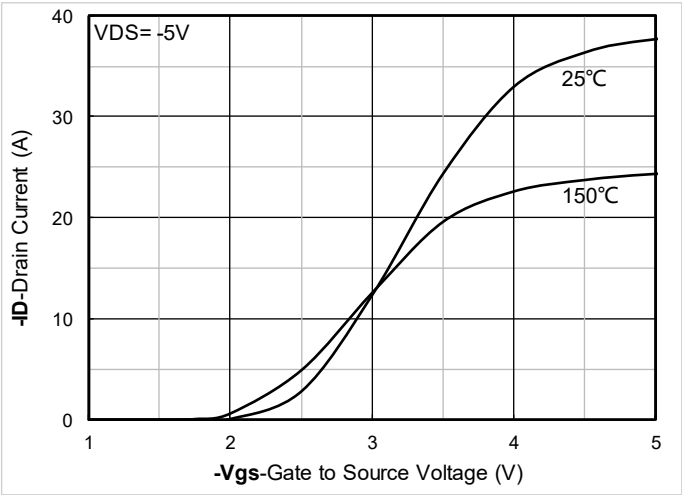


Figure 2. Transfer Characteristics

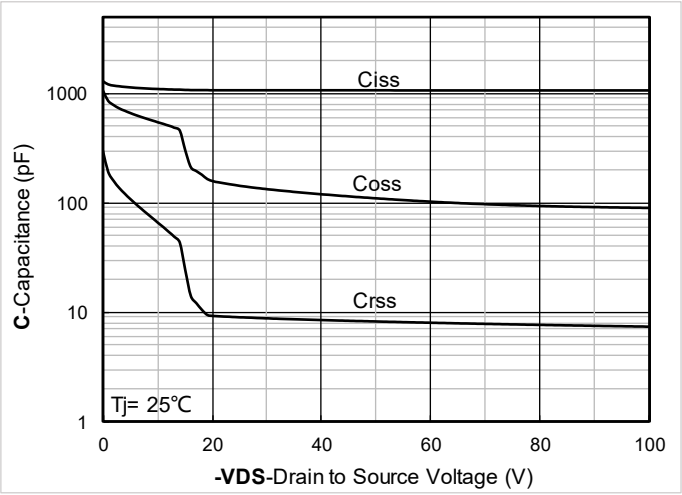


Figure 3. Capacitance Characteristics

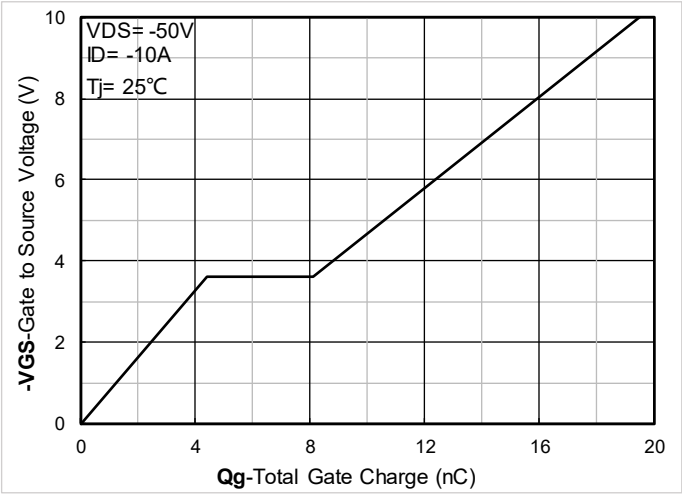


Figure 4. Gate Charge

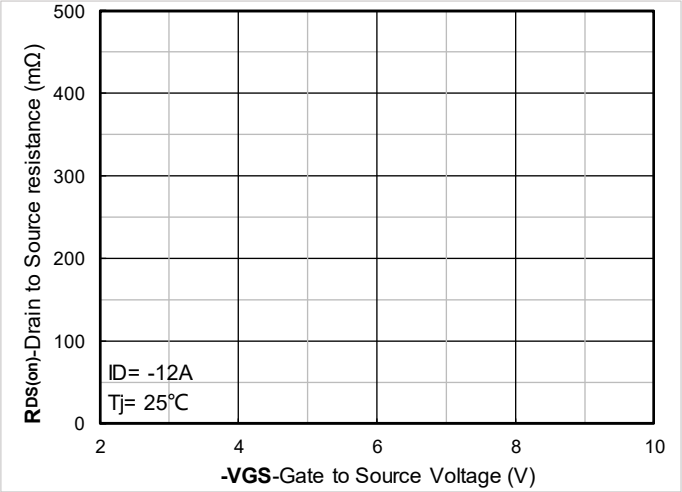


Figure 5. On-Resistance vs Gate to Source Voltage

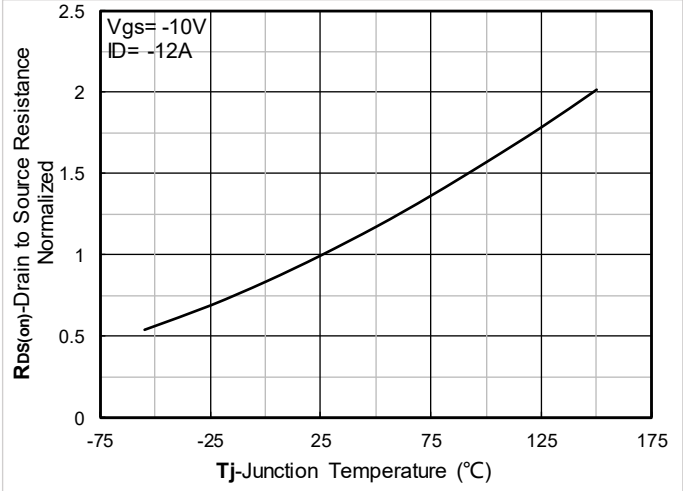


Figure 6. Normalized On-Resistance

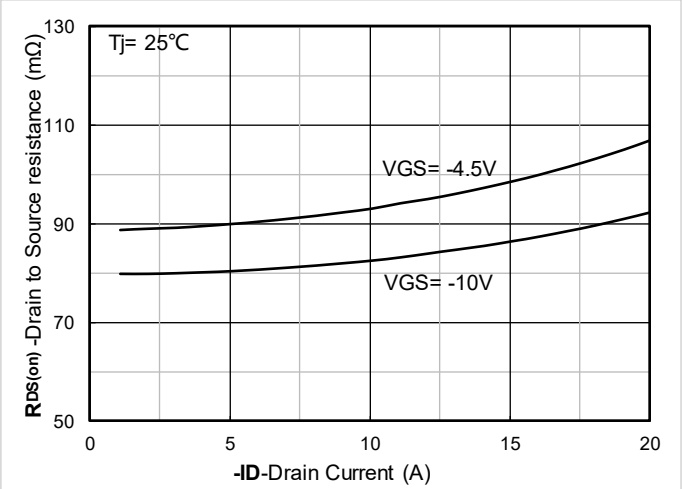


Figure 7. $R_{DS(on)}$ VS Drain Current

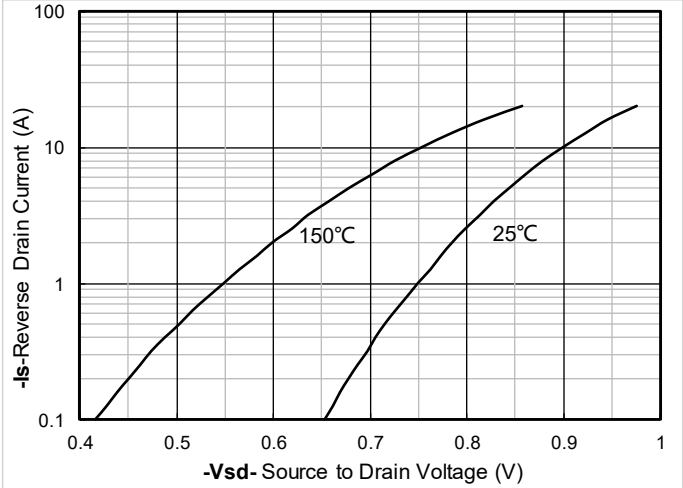


Figure 8. Forward characteristics of reverse diode

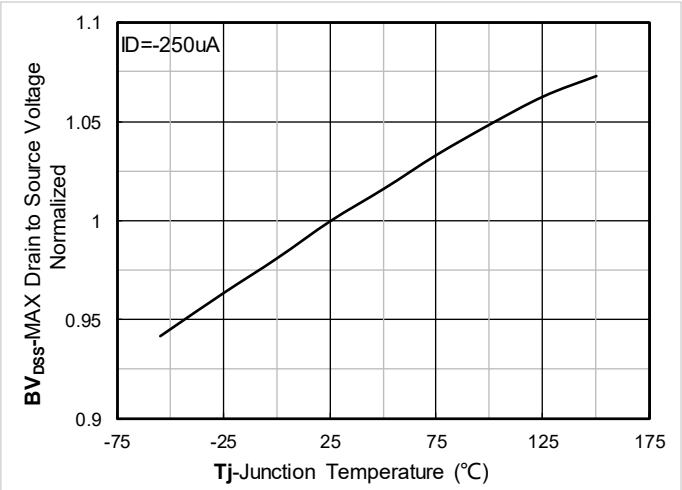


Figure 9. Normalized breakdown voltage

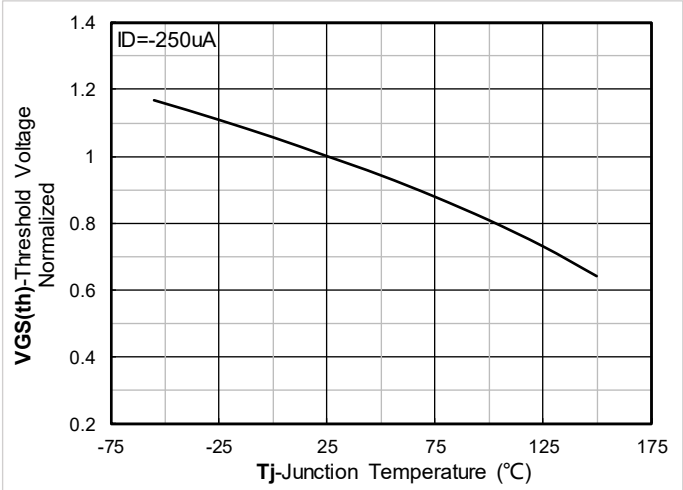


Figure 10. Normalized Threshold voltage

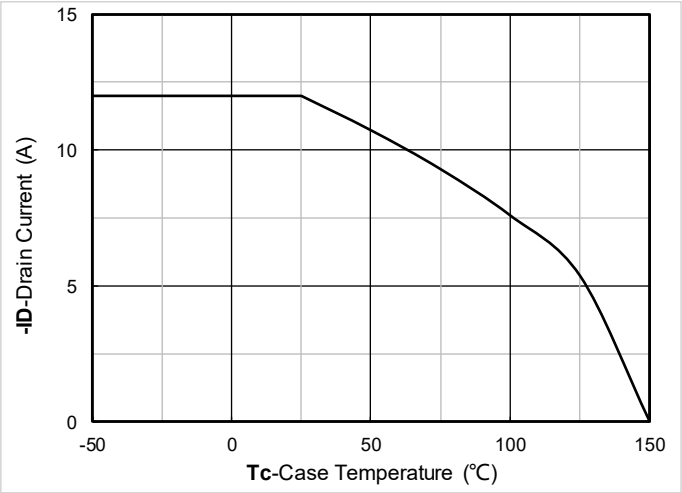


Figure 11. Current dissipation

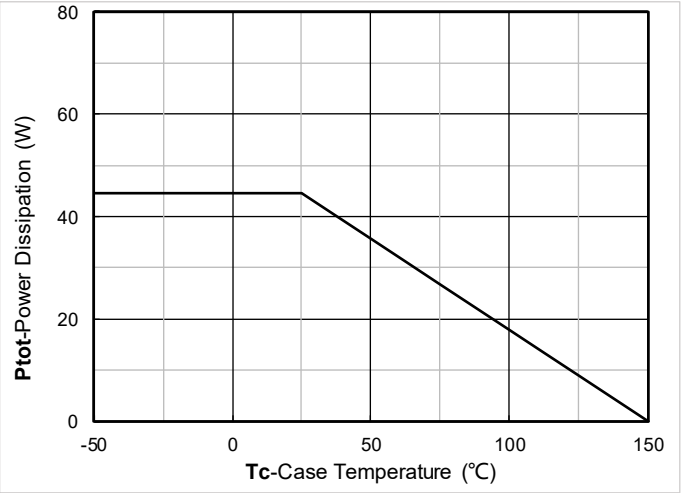


Figure 12. Power dissipation

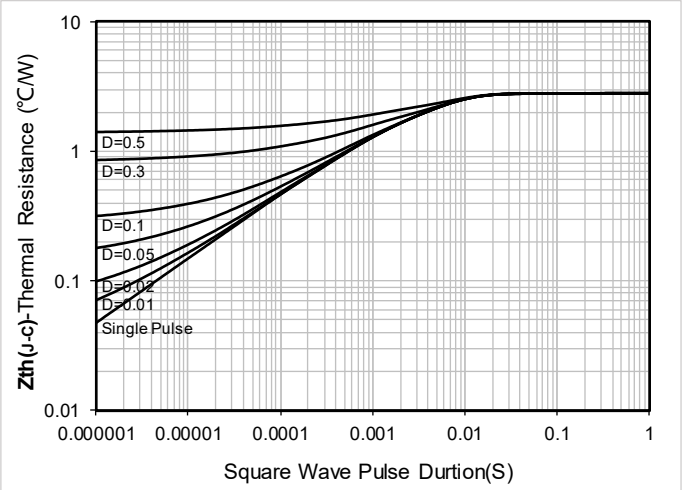


Figure 13. Maximum Transient Thermal Impedance

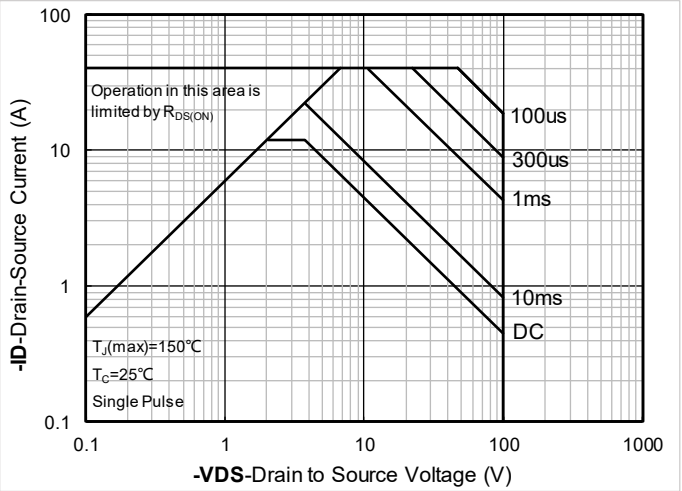
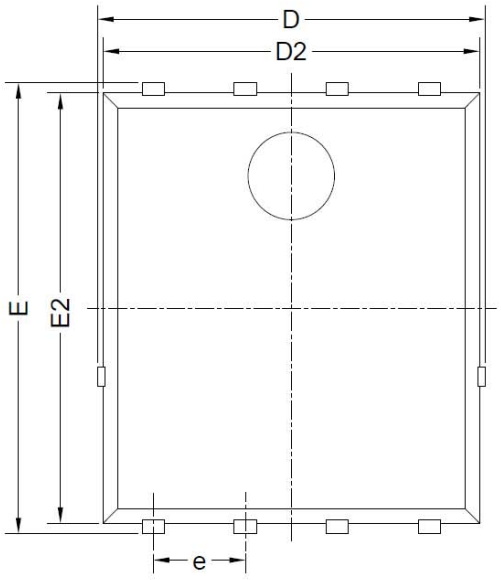
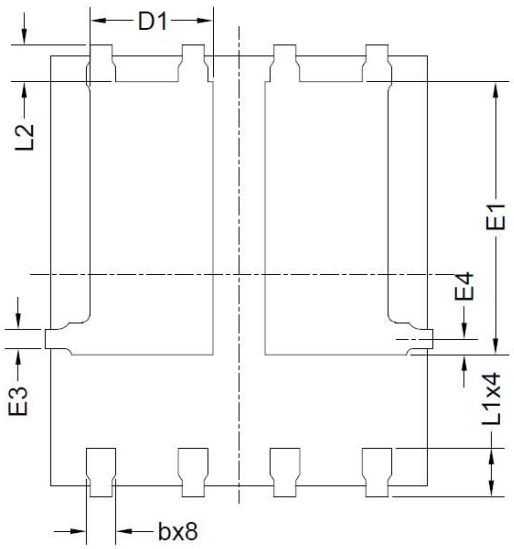


Figure 14. Safe Operation Area

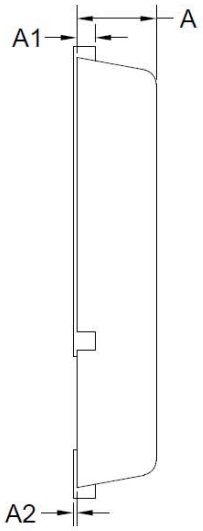
■ PDFN5060-8L-E-1.1MM Package information



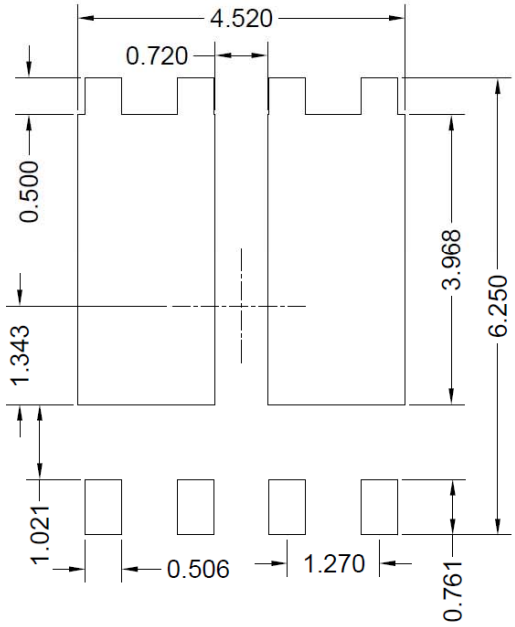
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254REF	
E4		0.21REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Notice

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