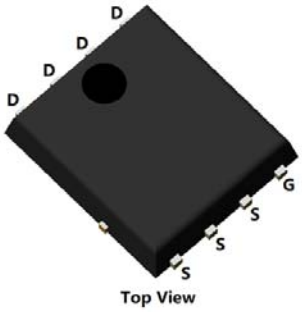
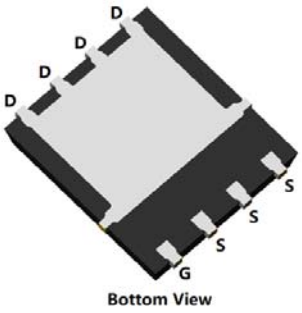
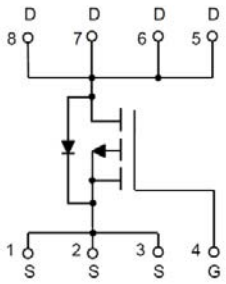
P-Channel Enhancement Mode Field Effect Transistor





PDFN5060-8L



Product Summary

- V_{DS} -100V
- I_D -15A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜110 mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜120 mohm
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	-3	A
	T_A=100℃		-2	
	T_C=25℃		-15	
	T_C=100℃		-9.6	
Pulsed Drain Current [A]		I_{DM}	-30	A
Avalanche energy [B]		E_{AS}	64	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2.5	W
	T_A=100℃		1	
	T_C=25℃		60	
	T_C=100℃		24	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t≤10S	$R_{\theta JA}$	15	20	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		40	50	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.7	2.1	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
G15GP10A	F1	G15GP10A	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA		-100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V	T_J=25℃			-1	μA
			T_J=55℃			-5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V				±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA		-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-15A			83	110	mΩ
		V_{GS}= -4.5V, I_D=-7A			95	120	
Diode Forward Voltage	V_{SD}	I_S=-15A,V_{GS}=0V				-1.3	V
Gate resistance	R_G	f=1MHz, Open drain		-	10	-	Ω
Maximum Body-Diode Continuous Current	I_S					-15	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=-50V,V_{GS}=0V,f=1MHZ			1051		pF
Output Capacitance	C_{oss}				119		
Reverse Transfer Capacitance	C_{rss}				25		
Switching Parameters							
Total Gate Charge	Q_g(-10V)	V_{GS}=-10V,V_{DS}=-50V,I_D=-5A			20.1		nC
Total Gate Charge	Q_g(-4.5V)				9.7		
Gate-Source Charge	Q_{gs}				3.9		
Gate-Drain Charge	Q_{gd}				4.3		
Reverse Recovery Chrage	Q_{rr}	I_F=-5A, di/dt=100A/us			140		
Reverse Recovery Time	t_{rr}				80		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-50V,I_{DS}=-5A R_{GEN}=6Ω			10		
Turn-on Rise Time	t_r				30		
Turn-off Delay Time	$t_{D(off)}$				77		
Turn-off fall Time	t_f				81		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. T_J=25℃, V_{DD}=-50V, V_G=-10V, R_G=25Ω, L=0.5mH, IAS=-16A.
C. Pd is based on max. junction temperature, using junction-case thermal resistance.
D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

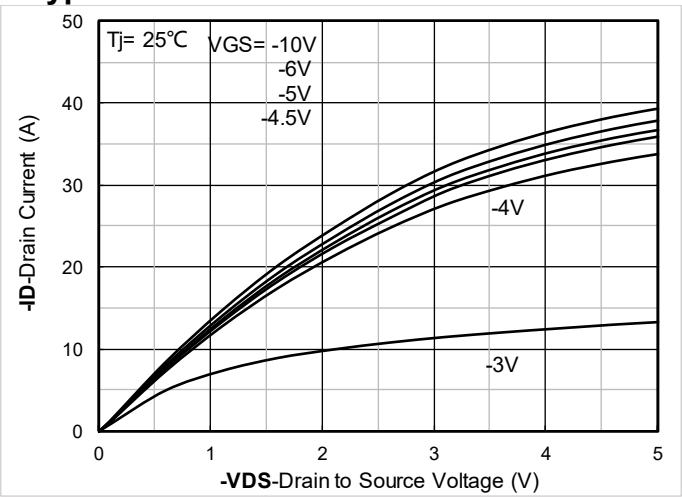


Figure1. Output Characteristics

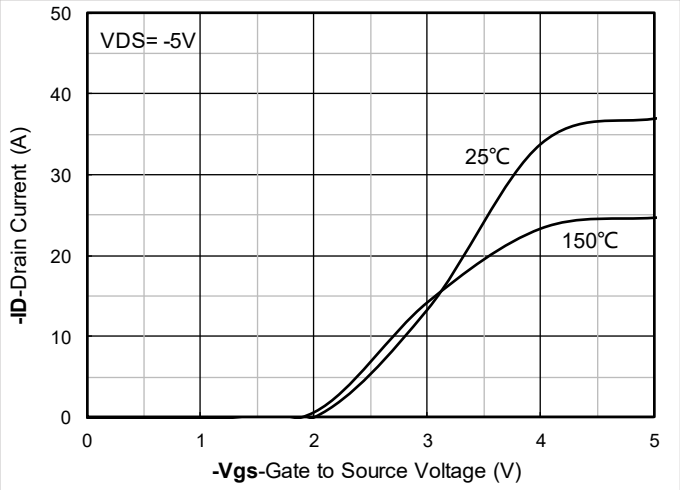


Figure2. Transfer Characteristics

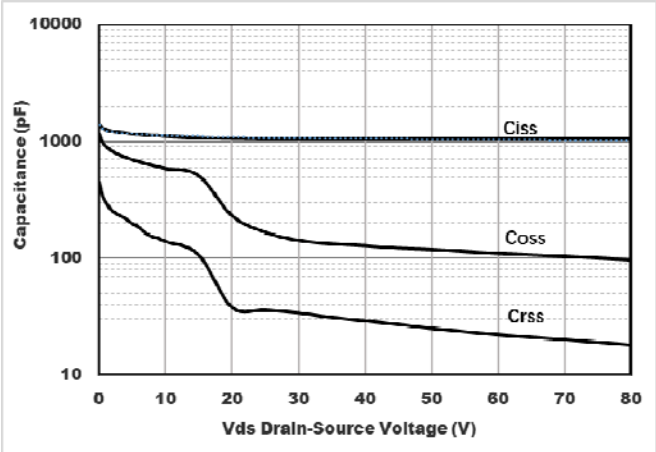


Figure3. Capacitance Characteristics

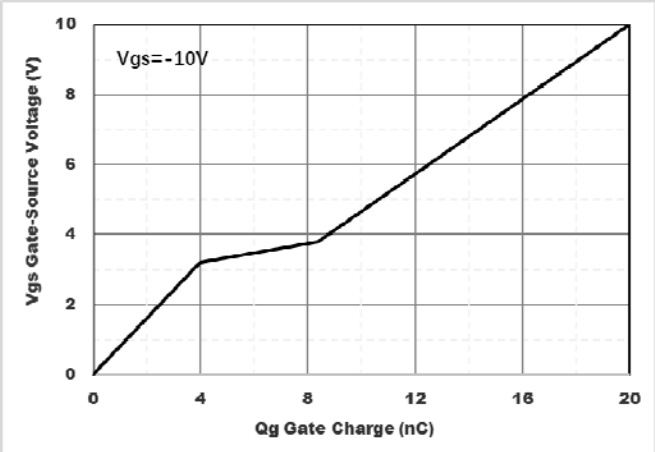


Figure4. Gate Charge

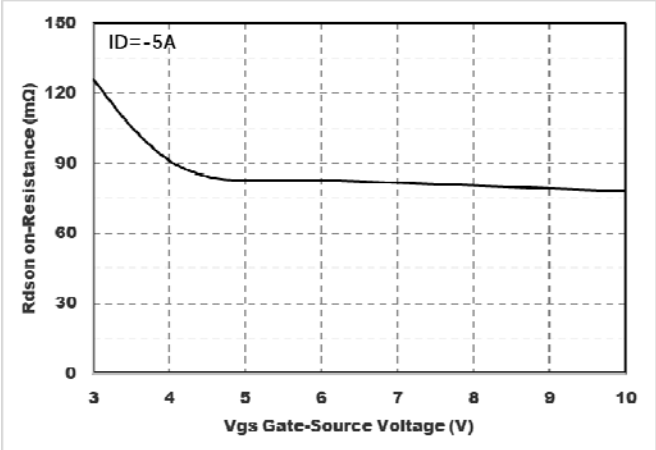


Figure5. : On-Resistance vs. Gate to Source Voltage

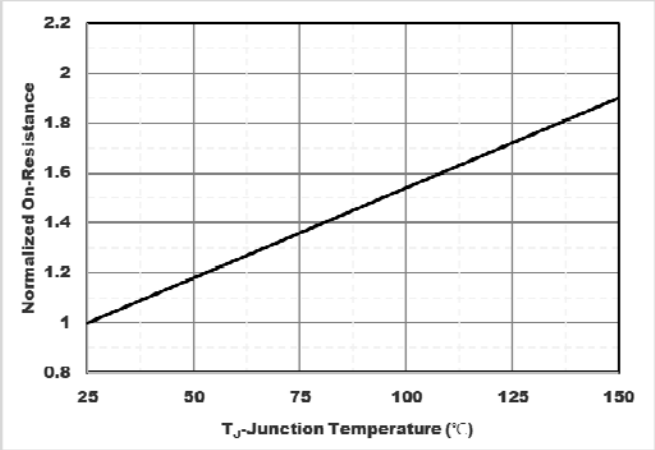


Figure6.Normalized On-Resistance

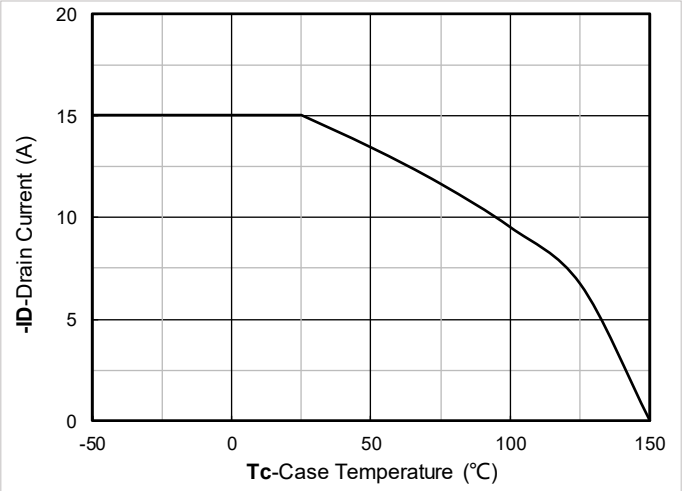


Figure7. Drain current

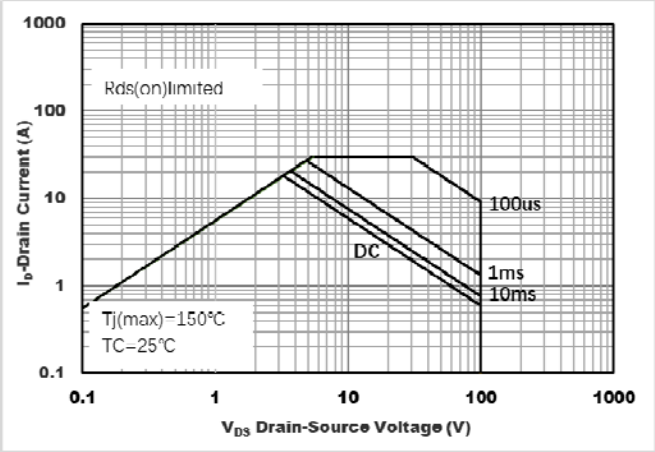


Figure8.Safe Operation Area

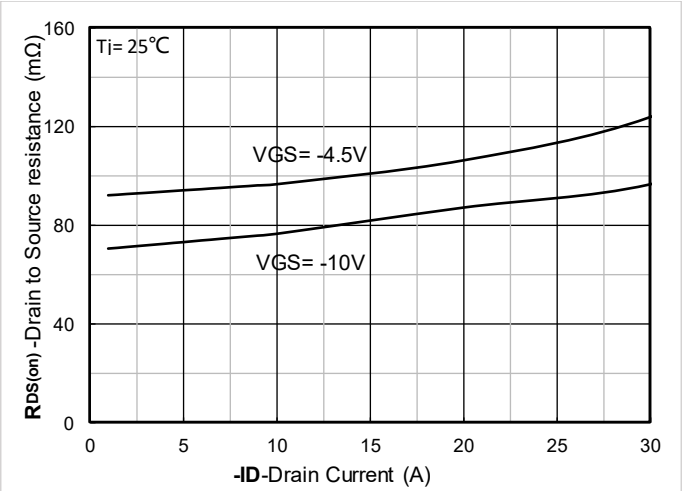


Figure 9. $R_{DS(on)}$ VS Drain Current

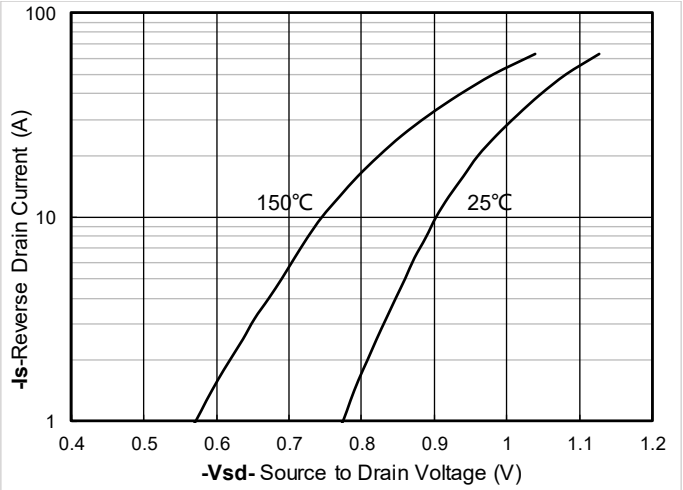


Figure 10. Forward characteristics of reverse diode

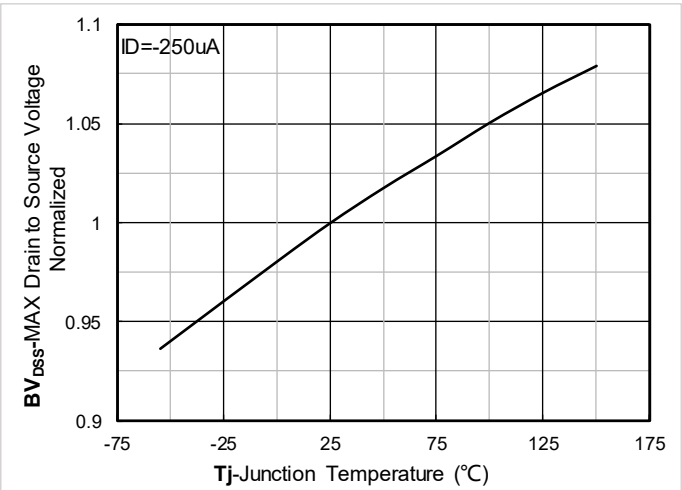


Figure 11. Normalized breakdown voltage

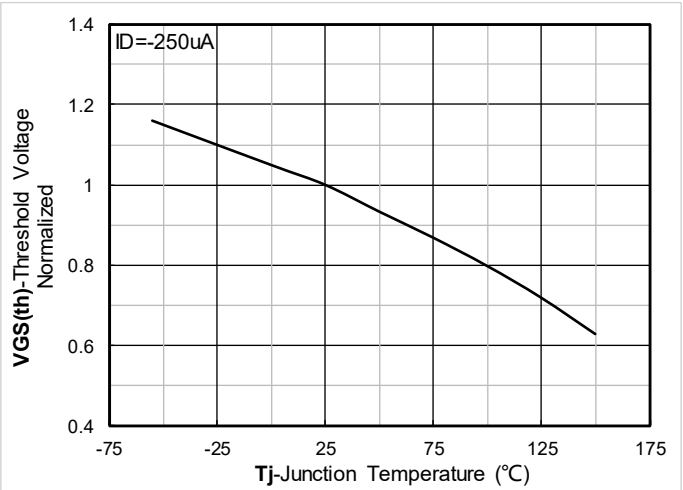


Figure 12. Normalized Threshold voltage

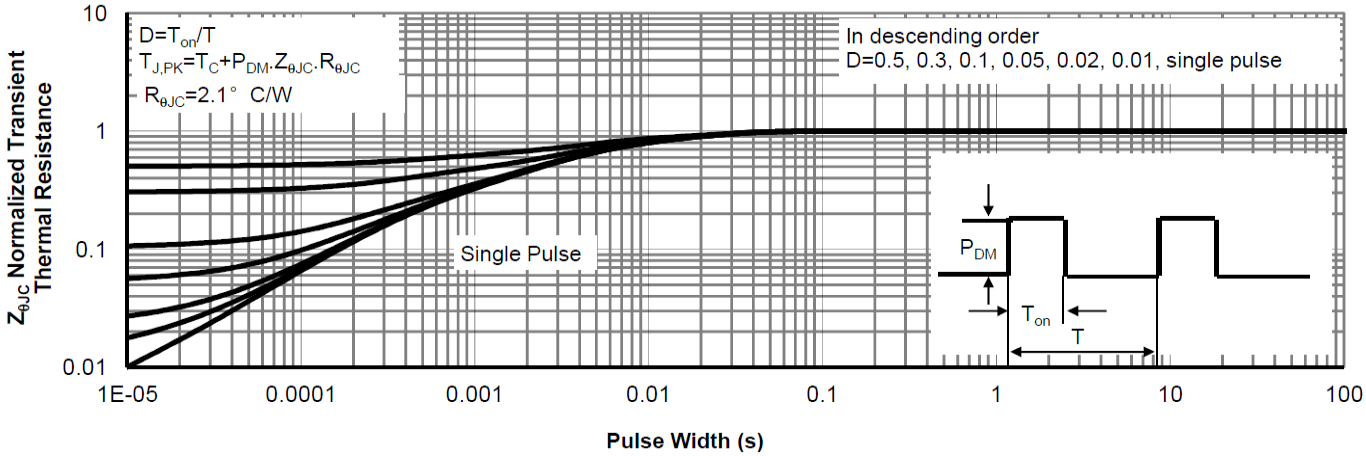
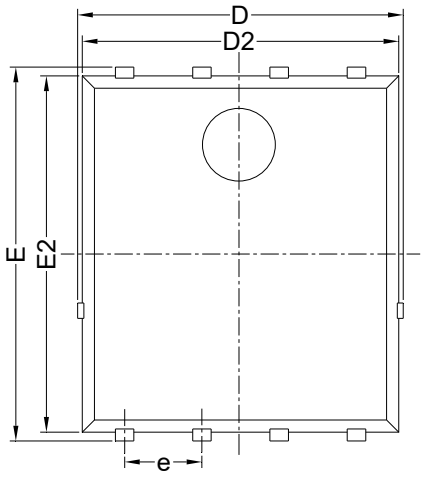
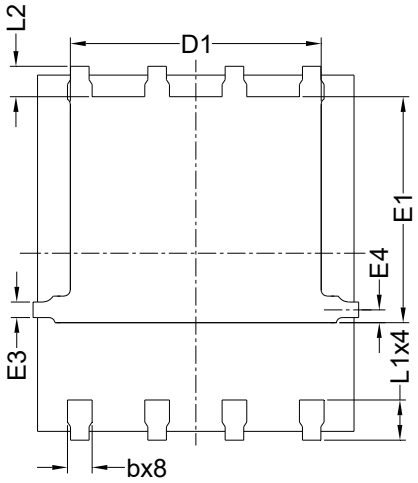


Figure13.Normalized Maximum Transient thermal impedance

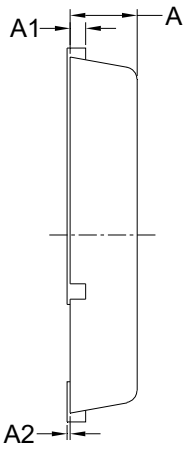
■ PDFN5060-8L-B-1.1MM Package Information



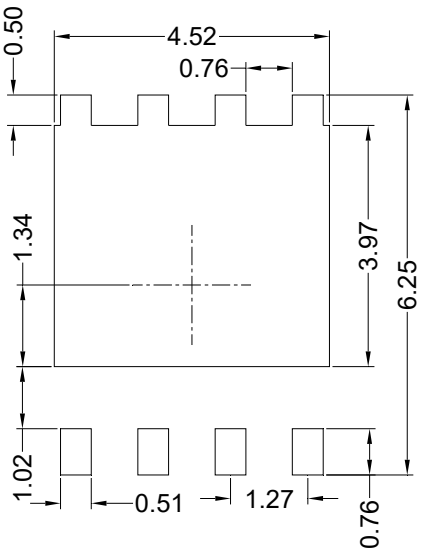
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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