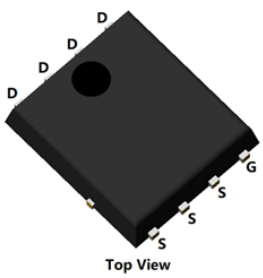
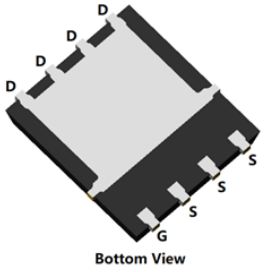
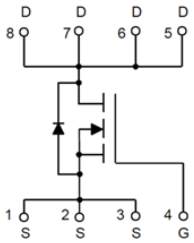
N-Channel Enhancement Mode Field Effect Transistor





PDFN5060-8L



Product Summary

- V_{DS} 100V
- I_D 114A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜6.2mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- 48V Port

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	100	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	14.3	A
		T_A=100℃,V_{GS}=10V		-	10.1	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V,Chip limitation		-	114	
		T_C=100℃,V_{GS}=10V		-	80.6	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	456	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		114	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=28.7A		EAS	-	205.9	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	2.72	W
		T_A=100℃		-	1.36	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	174.4	
		T_C=100℃		-	87.2	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	175	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	55	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.86	

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=1mA,Tj=25℃	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=100V,V_{GS}=0V,Tj=150℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2.2	3	3.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=50A,Tj=25℃	-	4.9	6.2	mΩ
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V,Tj=25℃	-	0.9	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	0.64	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHz,Tj=25℃	-	2735	-	pF
Output Capacitance	C_{oss}		-	923	-	
Reverse Transfer Capacitance	C_{rss}		-	23	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=50A,Tj=25℃	-	38.3	-	nC
Gate-Source Charge	Q_{gs}		-	12.8	-	
Gate-Drain Charge	Q_{gd}		-	7.6	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs,V_{GS}=0V,V_R=50V, Tj=25℃	-	35	-	nC
Reverse Recovery Time	t_{rr}		-	33.8	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=50V,I_D=50A,R_{GEN}=3Ω, Tj=25℃	-	17.9	-	ns
Turn-on Rise Time	t_r		-	6	-	
Turn-off Delay Time	$t_{D(off)}$		-	28.3	-	
Turn-off Fall Time	t_f		-	7.2	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

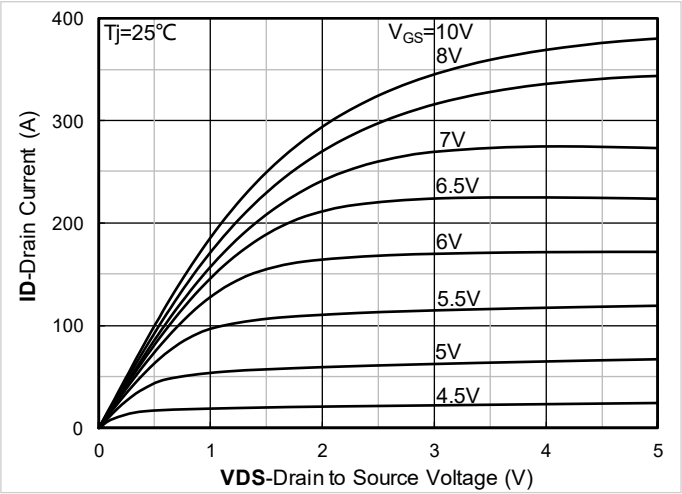


Figure 1. Output Characteristics; typical values

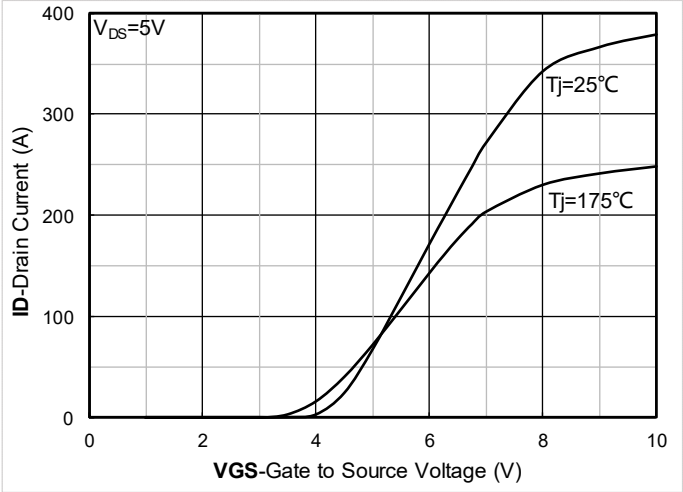


Figure 2. Transfer Characteristics; typical values

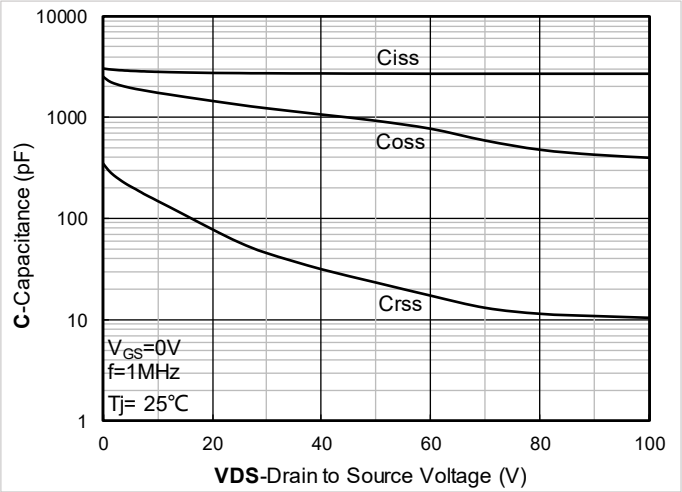


Figure 3. Capacitance Characteristics; typical values

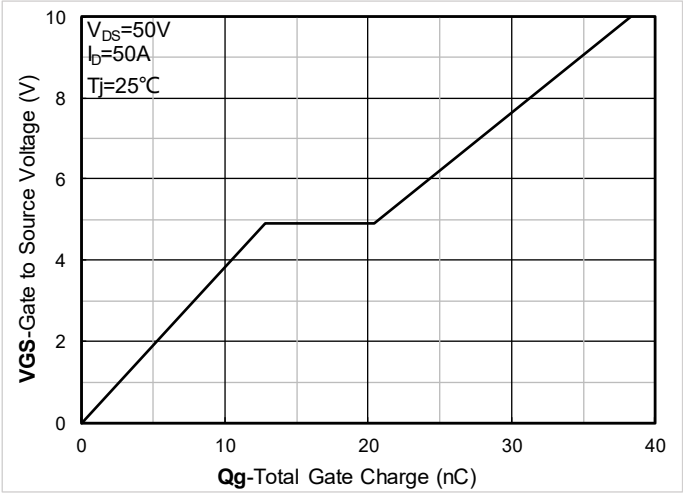


Figure 4. Gate Charge; typical values

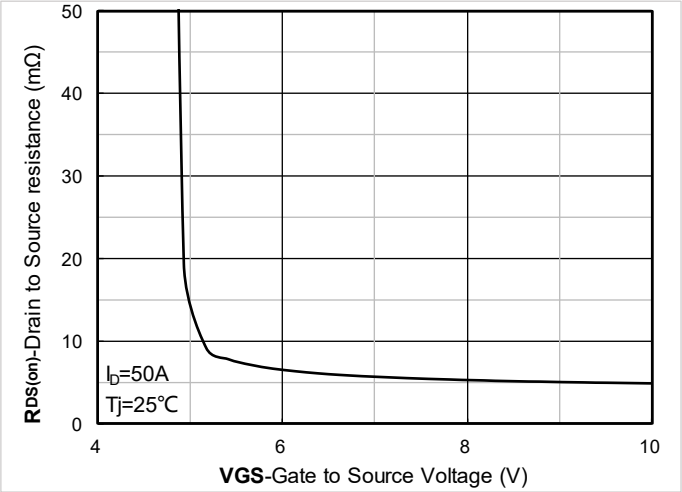


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

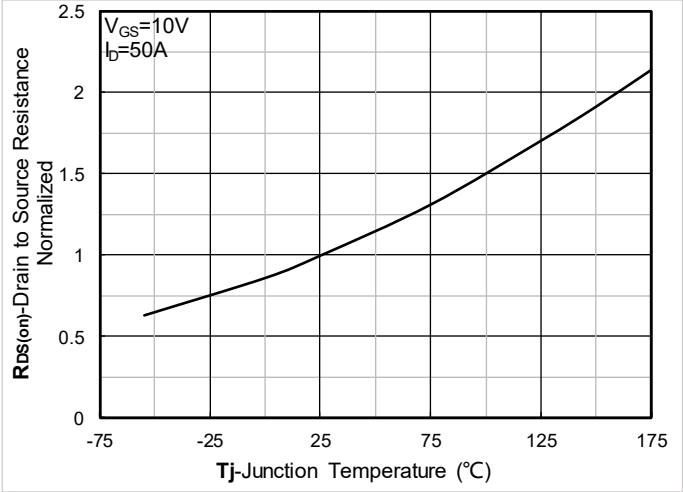


Figure 6. Normalized On-Resistance

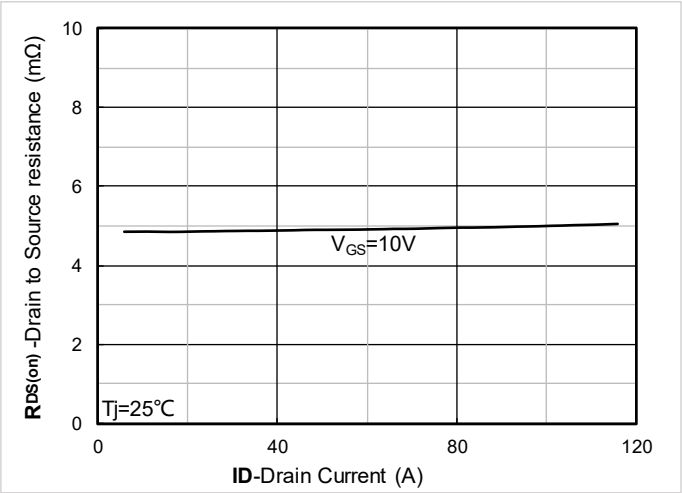


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

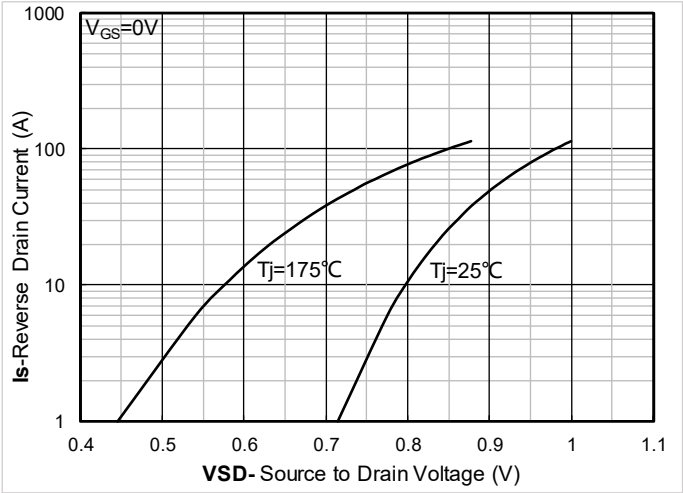


Figure 8. Forward characteristics of reverse diode; typical values

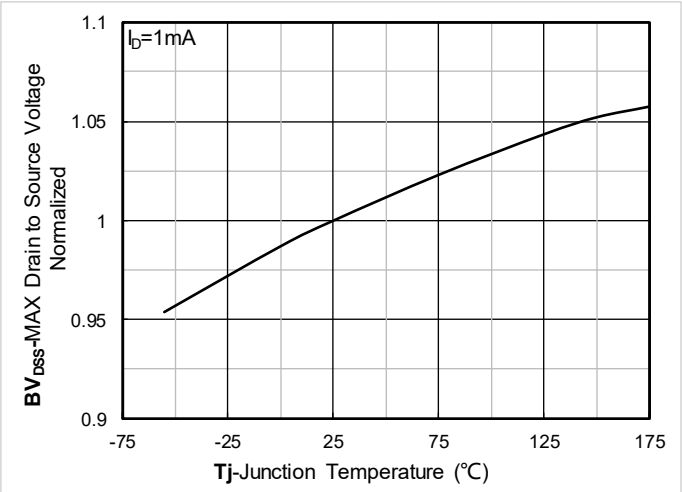


Figure 9. Normalized breakdown voltage

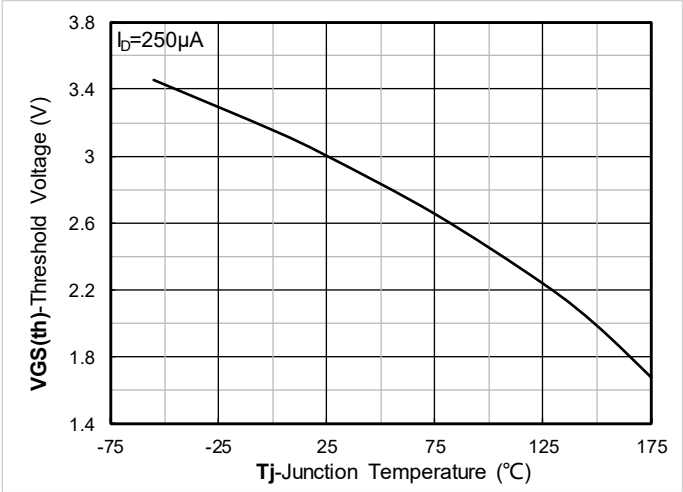


Figure 10. Gate Threshold voltage; typical values

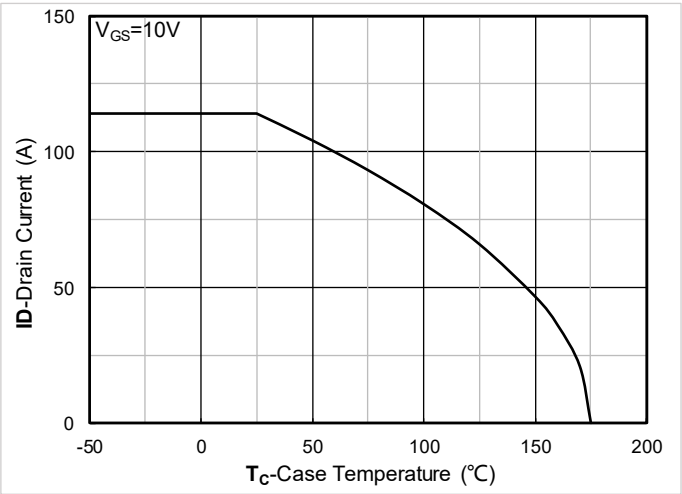


Figure 11. Current dissipation

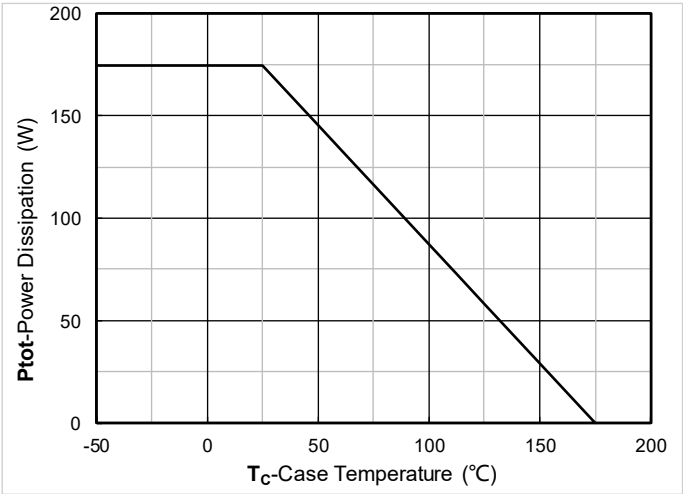


Figure 12. Power dissipation

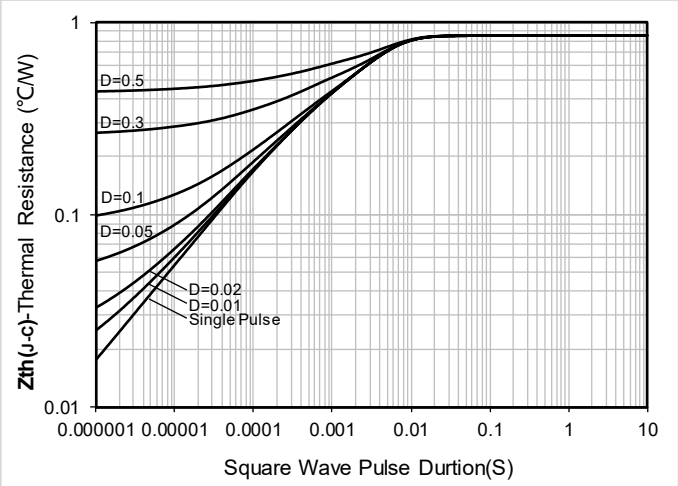


Figure 13. Maximum Transient Thermal Impedance

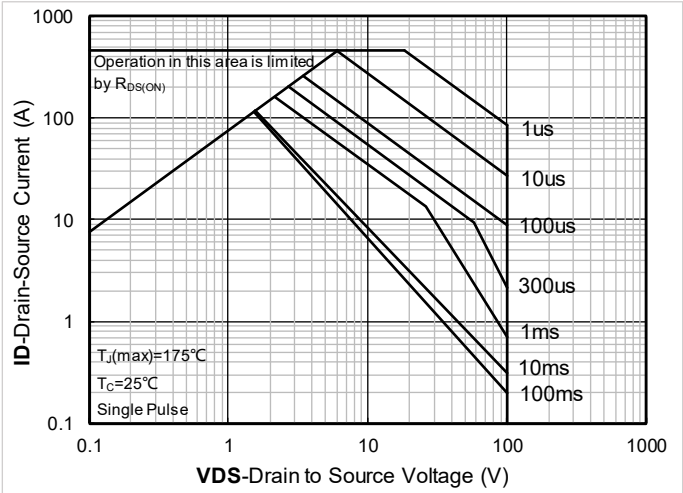
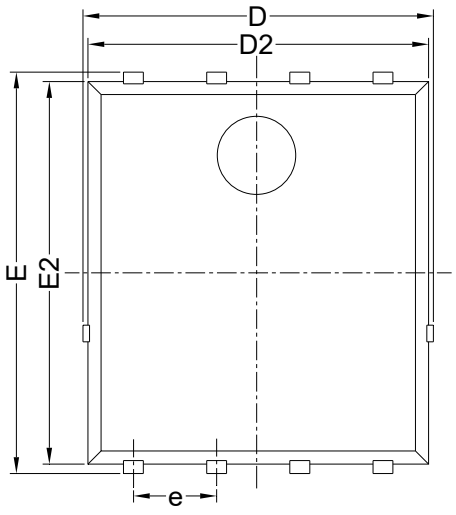
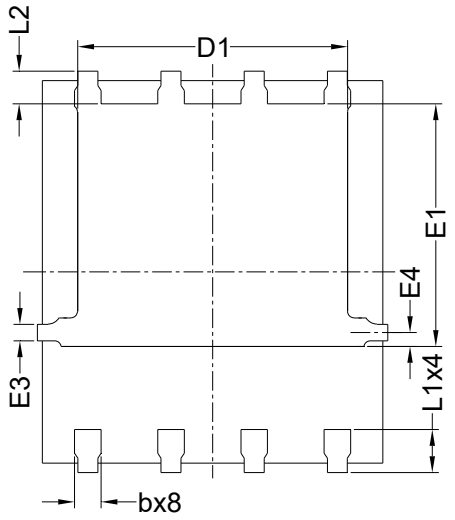


Figure 14. Safe Operation Area

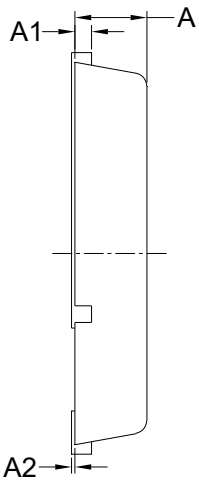
■ PDFN5060-8L-B-1.1MM Package information



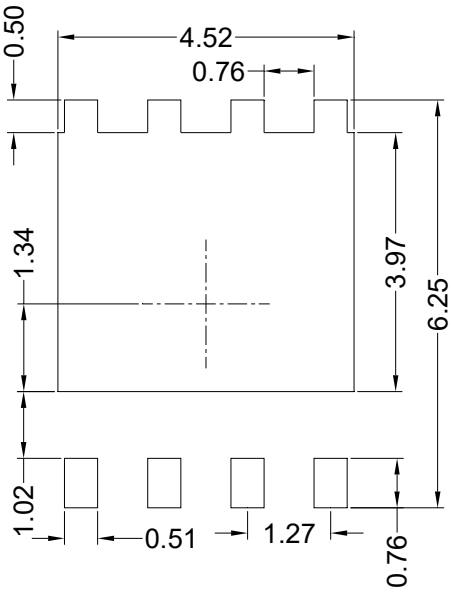
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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