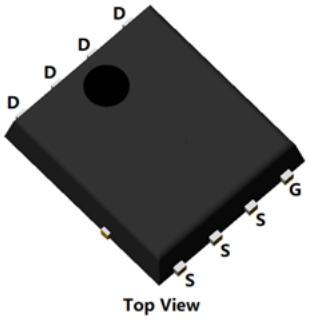
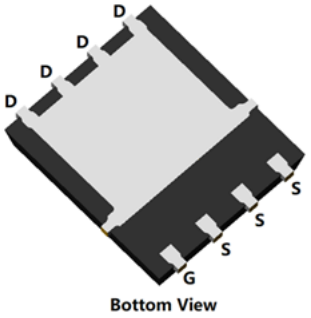
N-Channel Enhancement Mode Field Effect Transistor

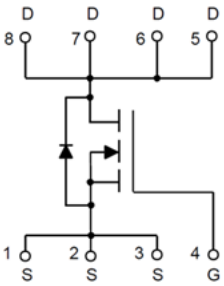


Top View



Bottom View

PDFN5060-8L



Product Summary

- V_{DS} 60V
- I_D 95A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜2.9 mohm
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current （Silicon limited）		I_D	155	A
Drain Current [A]	T_A=25℃	I_D	20	A
	T_A=100℃		12	
	T_C=25℃		95	
	T_C=100℃		60	
Pulsed Drain Current [B]		I_{DM}	390	A
Avalanche energy [C]		E_{AS}	800	mJ
Total Power Dissipation [D]		P_D	120	W
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.04	℃/ W
Thermal Resistance Junction-to-Ambient [E]		$R_{\theta JA}$	20	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
G95G06B	F1	G95G06B	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2.0	2.8	4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A		2.25	2.9	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				95	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=100KHz		5950		pF
Output Capacitance	C_{oss}			1250		
Reverse Transfer Capacitance	C_{rss}			85		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=50A		93		nC
Gate-Source Charge	Q_{gs}			17		
Gate-Drain Charge	Q_{gd}			14		
Reverse Recovery Chrage	Q_{rr}	I_F=25A, di/dt=100A/us		73		
Reverse Recovery Time	t_{rr}			68		ns
Turn-on Delay Time	$t_{d(on)}$	V_{GS}=10V,V_{DD}=30V,I_D=25A R_{GEN}=2Ω		22.5		
Turn-on Rise Time	t_r			6.7		
Turn-off Delay Time	$t_{d(off)}$			80.3		
Turn-off fall Time	t_f			26.9		

Note:

A. The maximum current rating is package limited.

B. Repetitive rating; pulse width limited by max. junction temperature.

C. T_J=25℃, V_{DD}=55V, V_G=10V, R_G=25Ω, L=4mH, IAS=20A.

D. P_D is based on max. junction temperature, using junction-case thermal resistance.

E. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25 ℃.

■ Typical Performance Characteristics

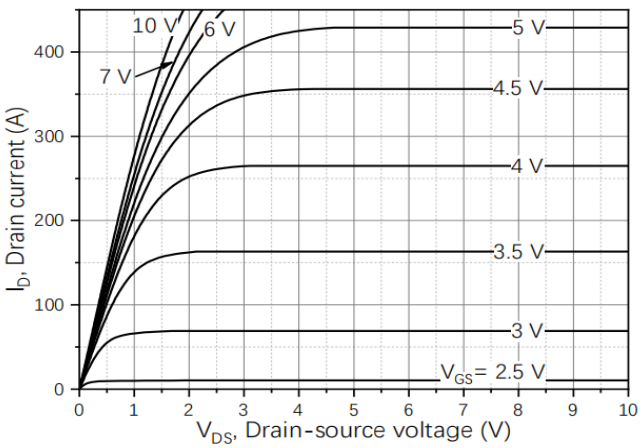


Figure1. Output Characteristics

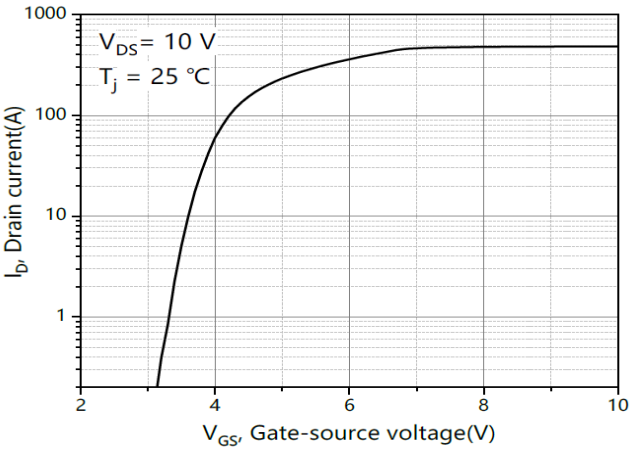


Figure2. Transfer Characteristics

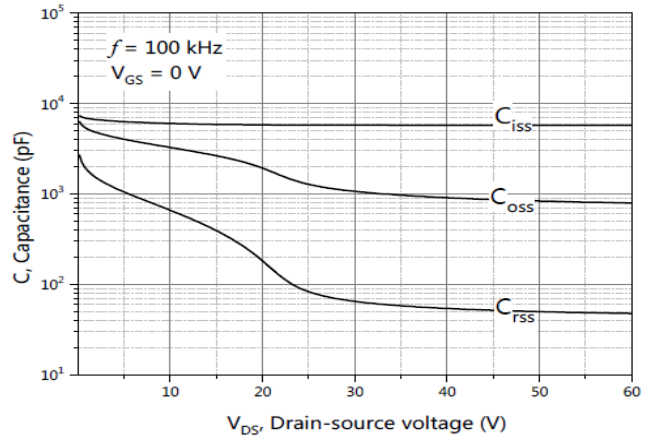


Figure3. Capacitance Characteristics

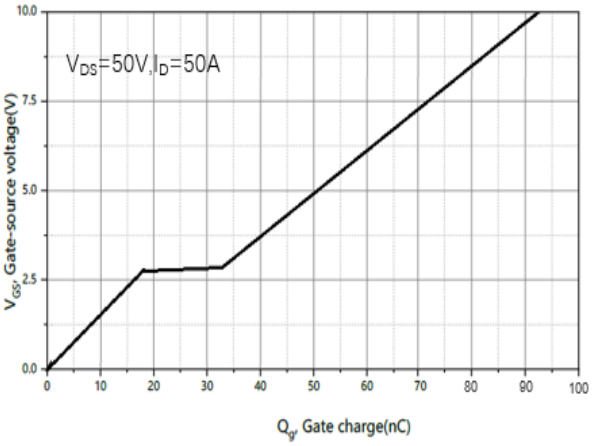


Figure4. Gate Charge

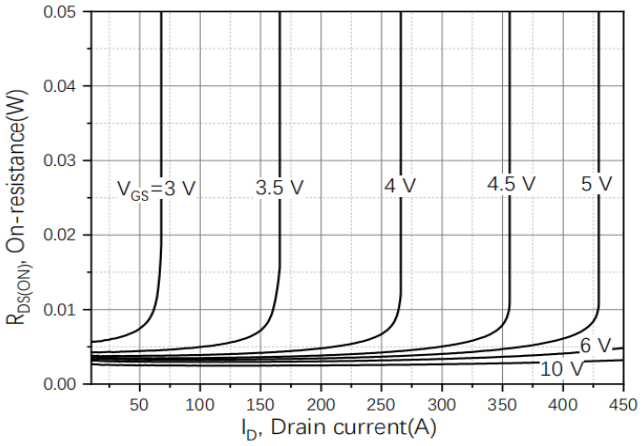


Figure5. Drain-Source on Resistance

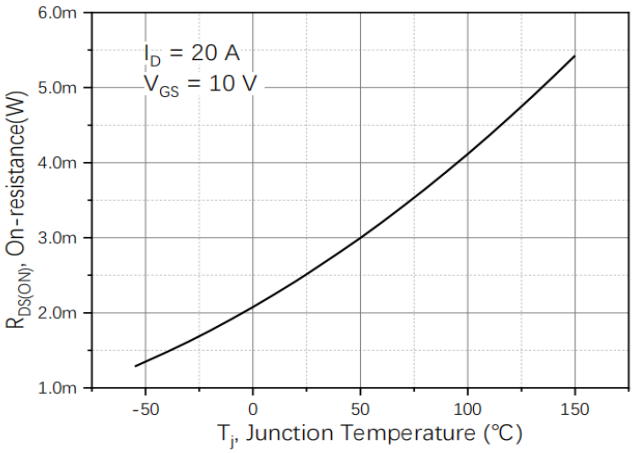


Figure6. Drain-Source on Resistance

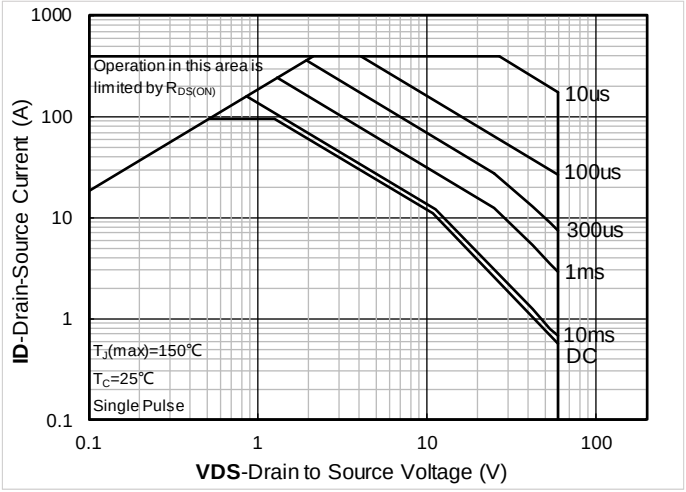


Figure7. Safe Operation Area

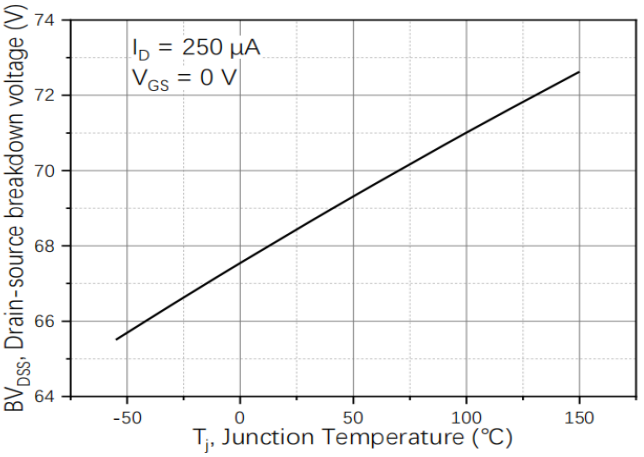


Figure8. Drain-source breakdown voltage

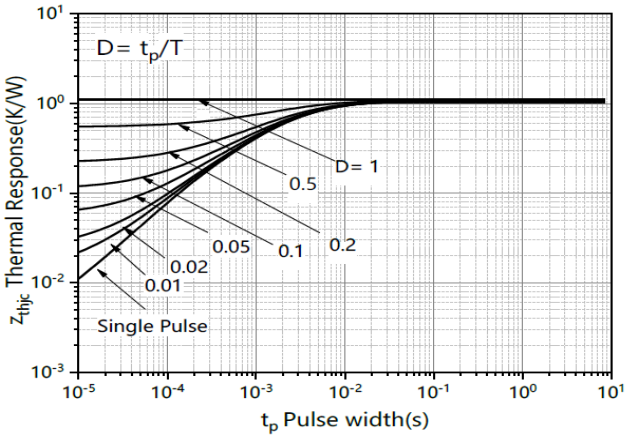
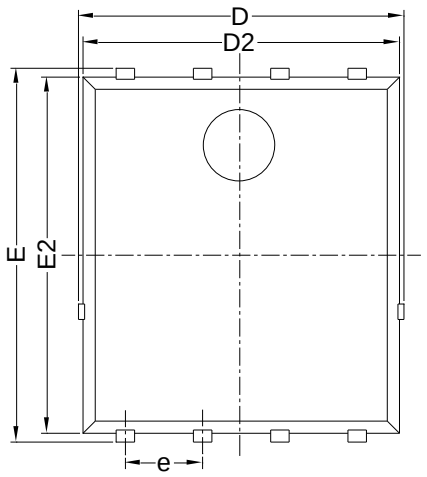
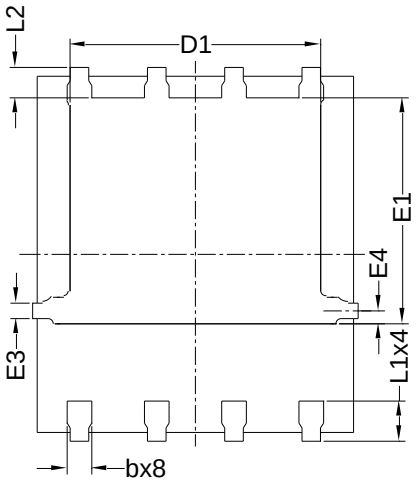


Figure 9.Transient thermal impedance

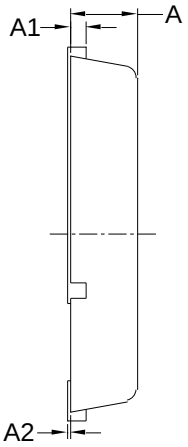
■ PDFN5060-8L-B-1.1MM Package Information



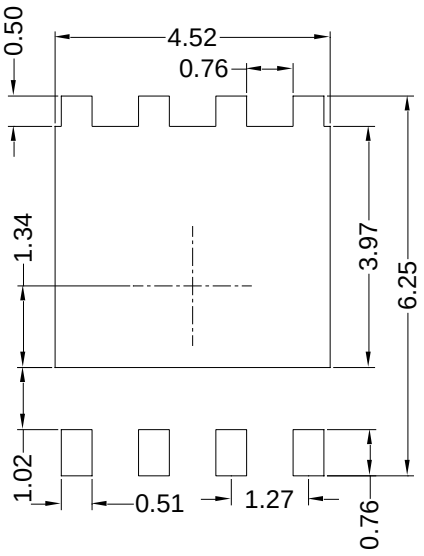
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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