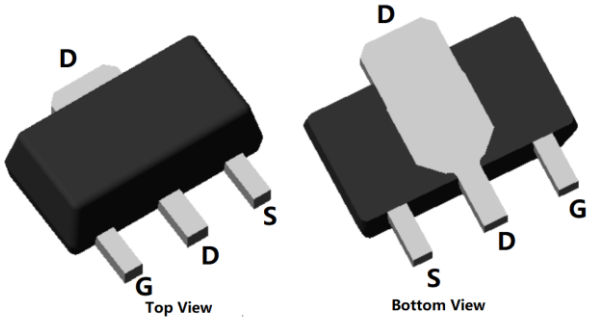
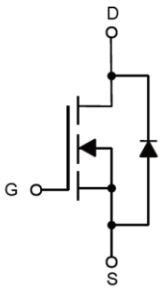
N-Channel Enhancement Mode Field Effect Transistor



SOT-89



Product Summary

- V_{DS} 60V
- I_D 3.0A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜100mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜120mohm

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	3	A
	T_A=70℃		2.4	
Pulsed Drain Current [A]		I_{DM}	12	A
Total Power Dissipation	T_A=25℃	P_D	0.69	W
	T_A=70℃		0.44	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	180	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
H03N06A	F2	6003A	1000	8000	32000	7“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS1}	V_{GS}=±20V, V_{DS}=0V			±100	nA
	I_{GSS2}	V_{GS}=±10V, V_{DS}=0V			±50	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.3	2.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=3A		86	100	mΩ
		V_{GS}=4.5V, I_D=2A		92	120	
Diode Forward Voltage	V_{SD}	I_S=3A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		409		pF
Output Capacitance	C_{oss}			50		
Reverse Transfer Capacitance	C_{rss}			41		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=30V,I_D=3A		10.27		nC
Gate-Source Charge	Q_{gs}			1.65		
Gate-Drain Charge	Q_{gd}			2.11		
Reverse Recovery Chrage	Q_{rr}	I_F=3A, di/dt=100A/us		6.99		
Reverse Recovery Time	t_{rr}			32.6		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DS}=30V, R_L=20Ω R_{GEN}=3Ω		3.6		
Turn-on Rise Time	t_r			17.6		
Turn-off Delay Time	$t_{D(off)}$			13		
Turn-off fall Time	t_f			23		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

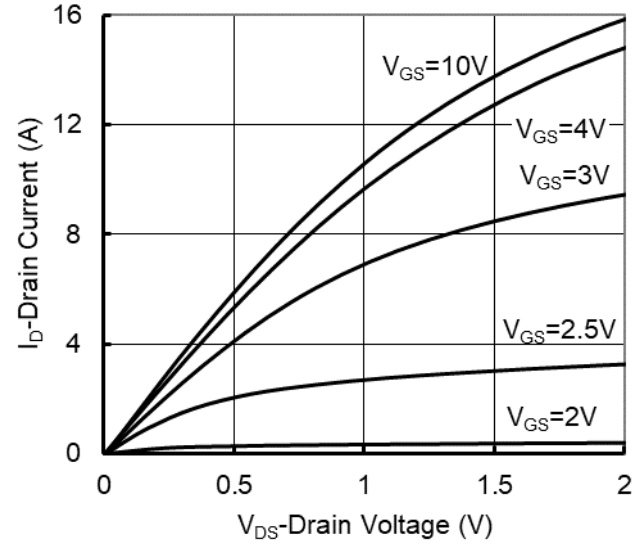


Figure1. Output Characteristics

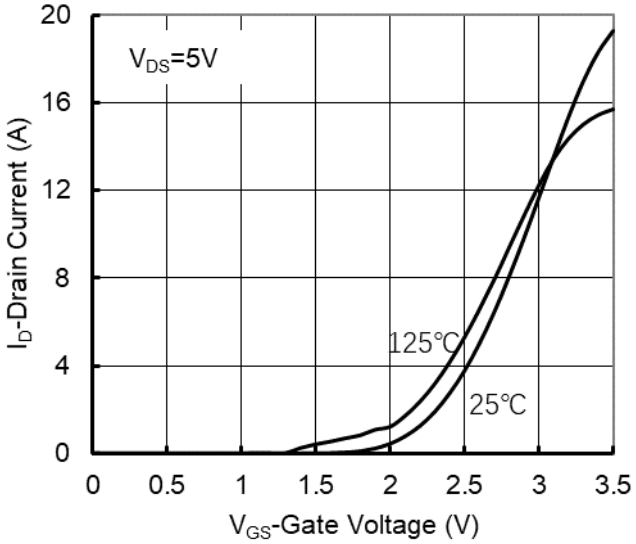


Figure2. Transfer Characteristics

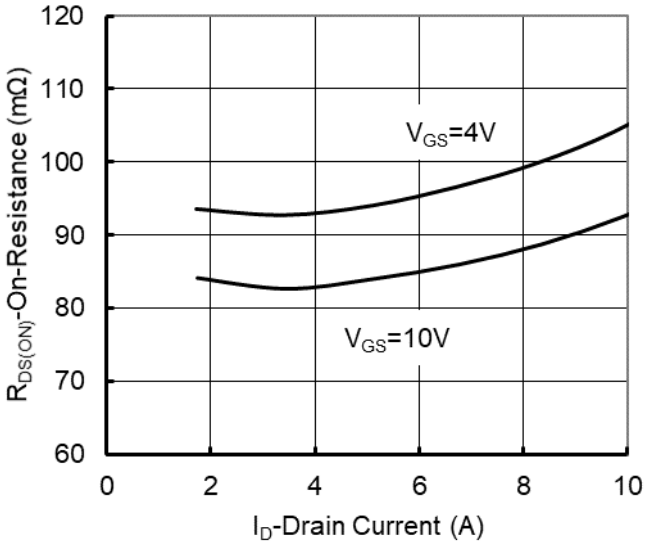


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

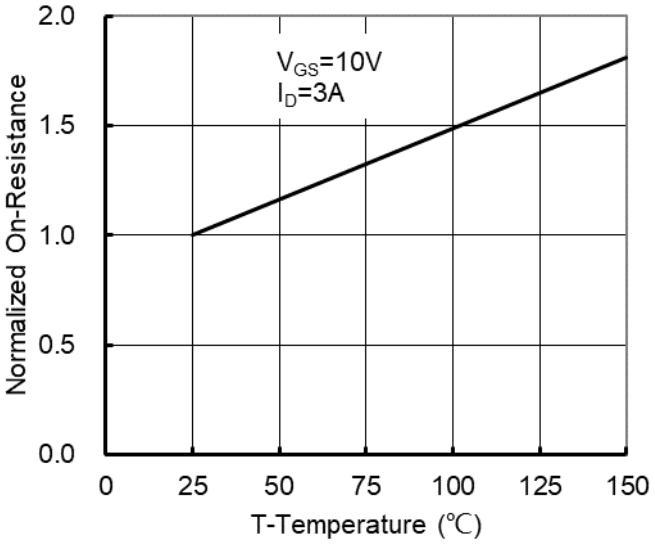


Figure 4: On-Resistance vs. Junction Temperature

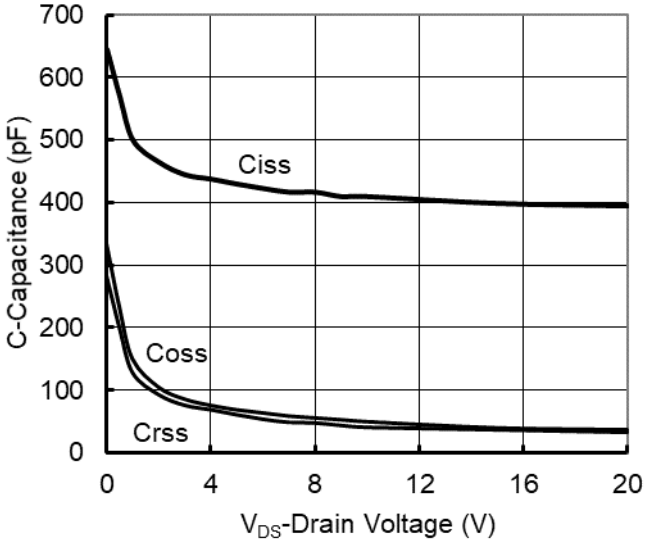


Figure5. Capacitance Characteristics

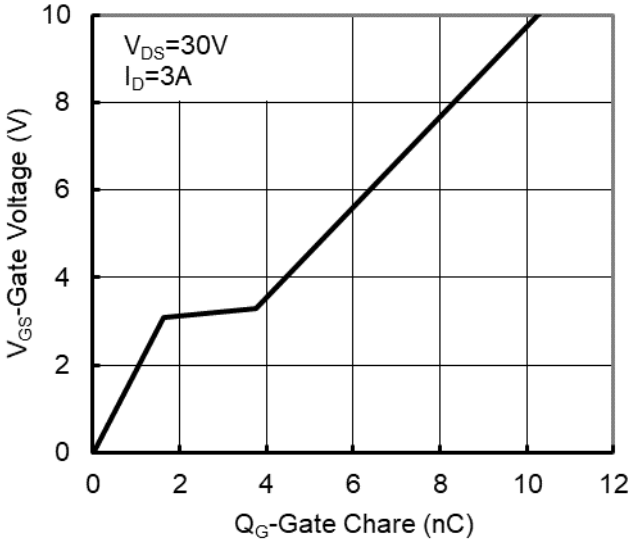


Figure6. Gate Charge

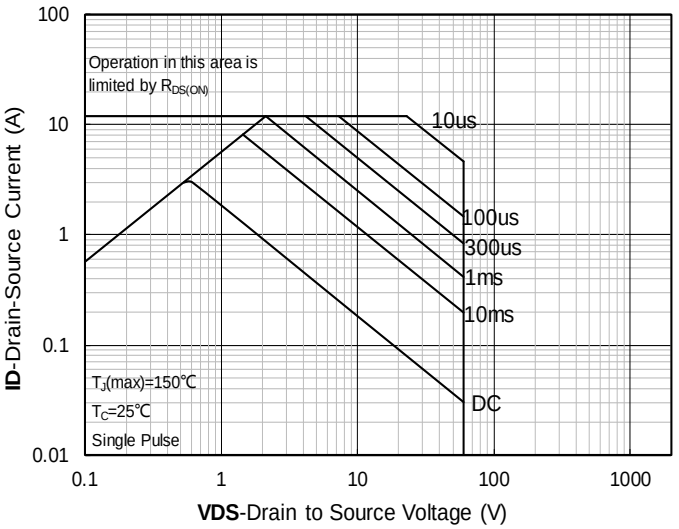


Figure7. Safe Operation Area

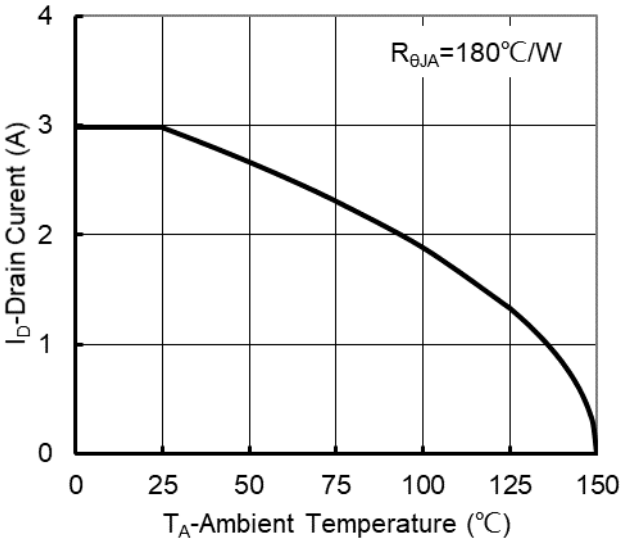


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

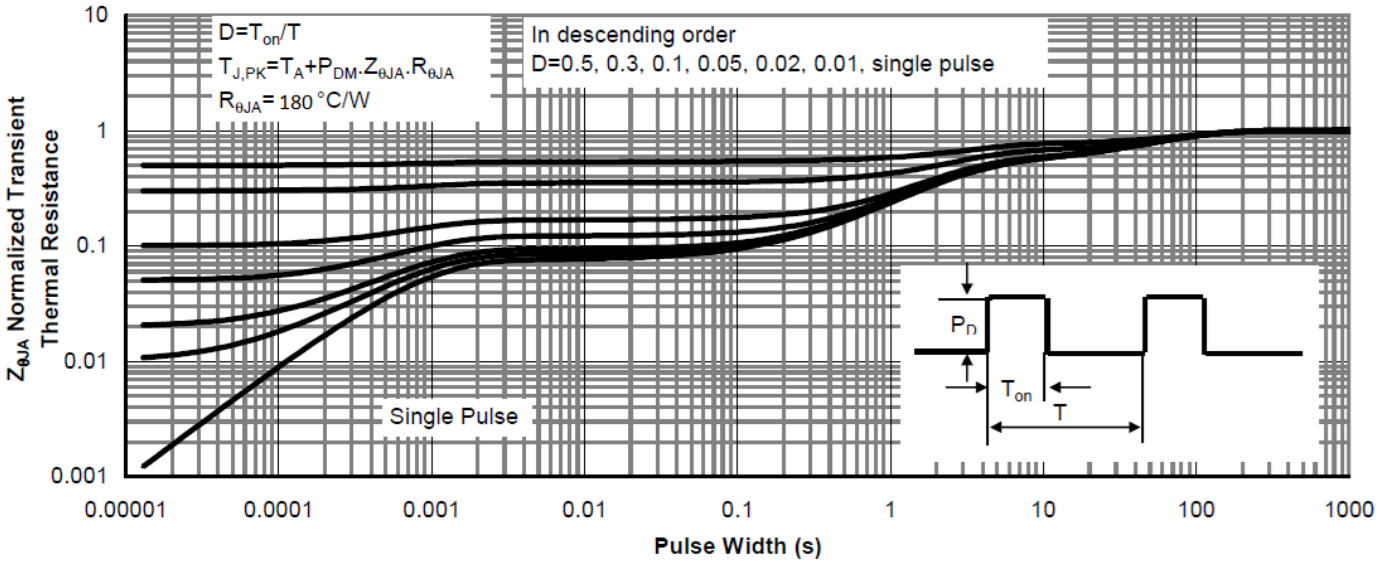
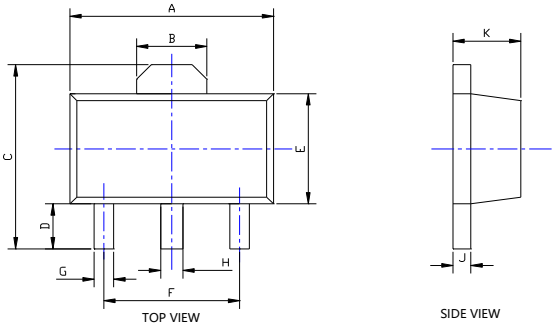
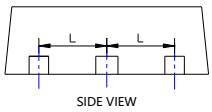
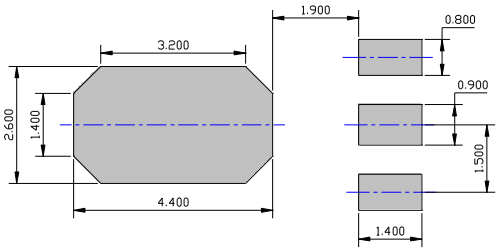


Figure9. Normalized Maximum Transient Thermal Impedance

■ SOT-89 Package Information







SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
DIM	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.169	0.185	4.300	4.700
B	0.061TYP		1.550TYP	
C	0.154	0.171	3.910	4.350
D	0.031	0.047	0.800	1.200
E	0.089	0.104	2.250	2.650
F	0.118TYP		3.000TYP	
G	0.013	0.020	0.330	0.520
H	0.016	0.023	0.400	0.580
J	0.014	0.017	0.350	0.440
K	0.055	0.063	1.400	1.600
L	0.059TYP		1.500TYP	

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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