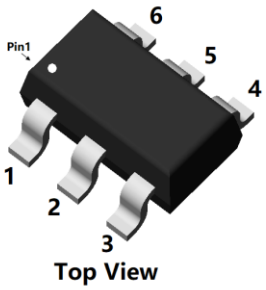
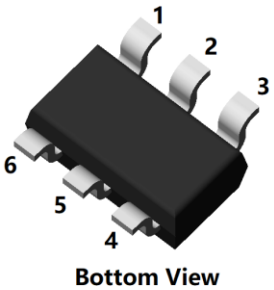
N-Channel Enhancement Mode Field Effect Transistor

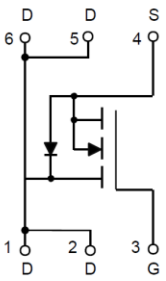


Top View



Bottom View

SOT-23-6L



Product Summary

- V_{DS} 60V
- I_D 5.0A
- $R_{DS(ON)}$(at V_{GS}= 10V) ＜ 43mohm
- $R_{DS(ON)}$(at V_{GS}= 4.5V) ＜ 47mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- PWM application
- Load switch

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃ @ Steady State	I_D	5.0	A
	T_A=70℃ @ Steady State		4.0	
	T_A=100℃ @ Steady State		3.1	
Pulsed Drain Current [A]		I_{DM}	20	A
Total Power Dissipation @ T_A=25℃		P_D	1.25	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]		$R_{\theta JA}$	100	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
J05N06A	F2	0605	3000	30000	120000	7“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=5.0A		34	43	mΩ
		V_{GS}= 4.5V, I_D=4.0A		36	47	
Diode Forward Voltage	V_{SD}	I_S=5.0A,V_{GS}=0V		0.8	1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V,f=1MHZ		1018		pF
Output Capacitance	C_{oss}			70		
Reverse Transfer Capacitance	C_{rss}			62		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=30V,I_D=10A		26.4		nC
Gate Source Charge	Q_{gs}			5.4		
Gate Drain Charge	Q_{gd}			6.5		
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=500A/us		11.7		
Reverse Recovery Time	t_{rr}			23		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=30V, I_D=2A,R_L=1Ω R_{GEN}=3Ω		10		
Turn-on Rise Time	t_r			20		
Turn-off Delay Time	$t_{D(off)}$			29		
Turn-off Fall Time	t_f			21		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

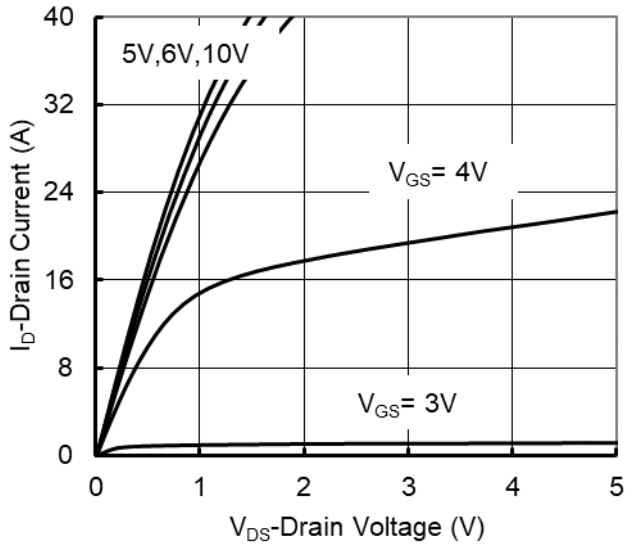


Figure 1. Output Characteristics

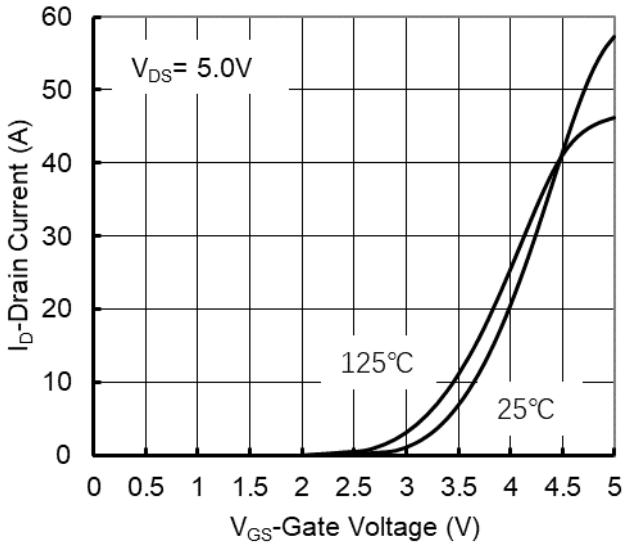


Figure 2. Transfer Characteristics

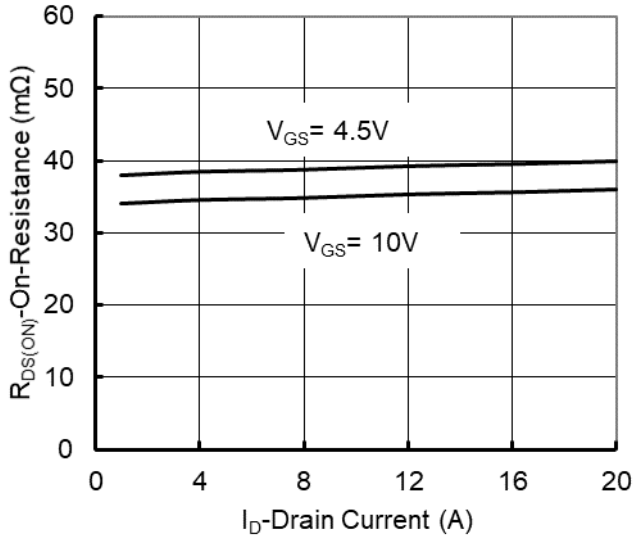


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

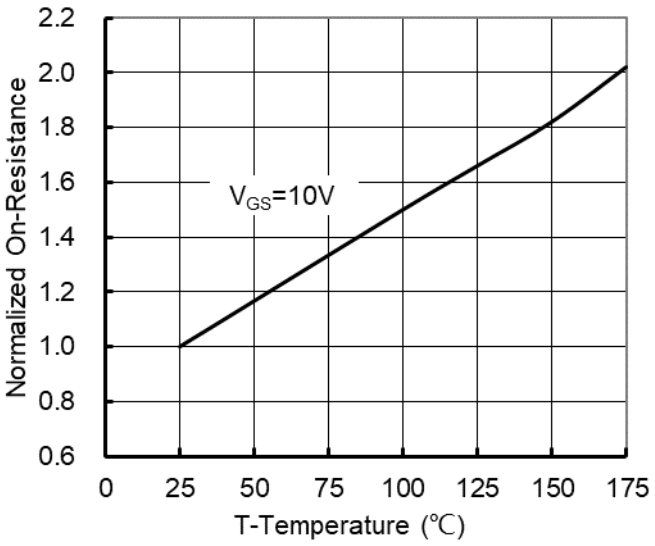


Figure 4. On-Resistance vs. Junction Temperature

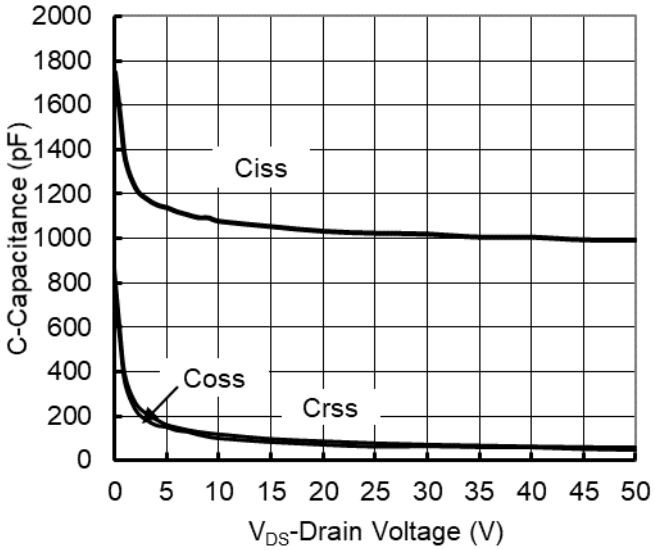


Figure 5. Capacitance Characteristics

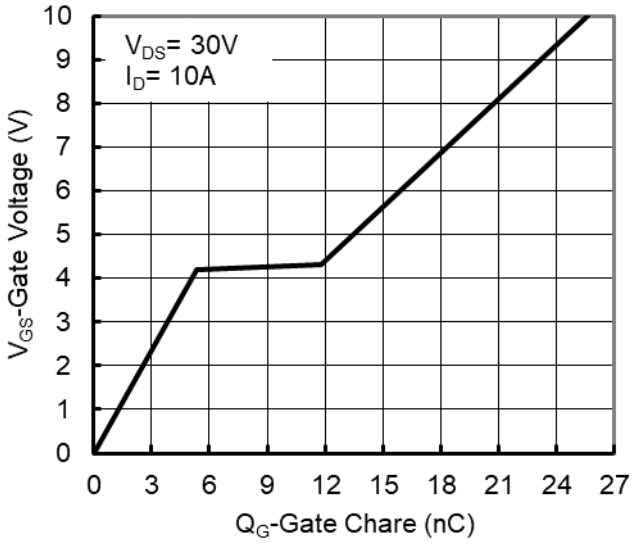


Figure 6. Gate Charge

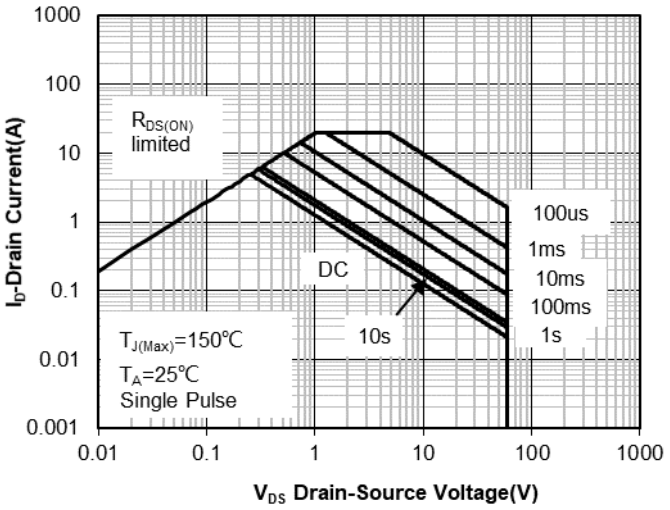


Figure 7. Safe Operation Area

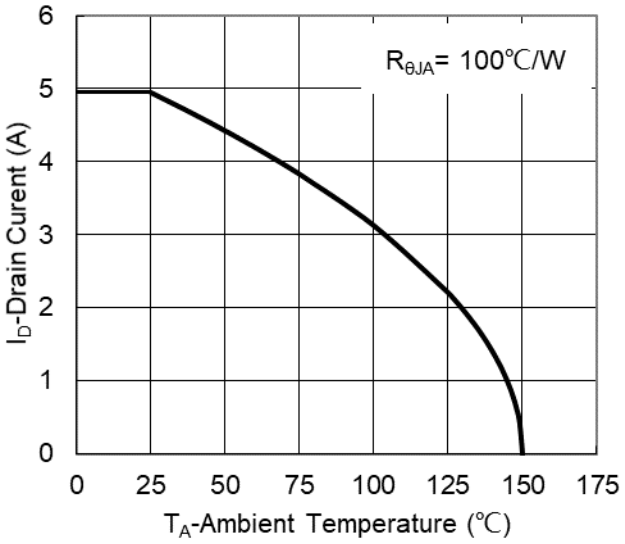


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

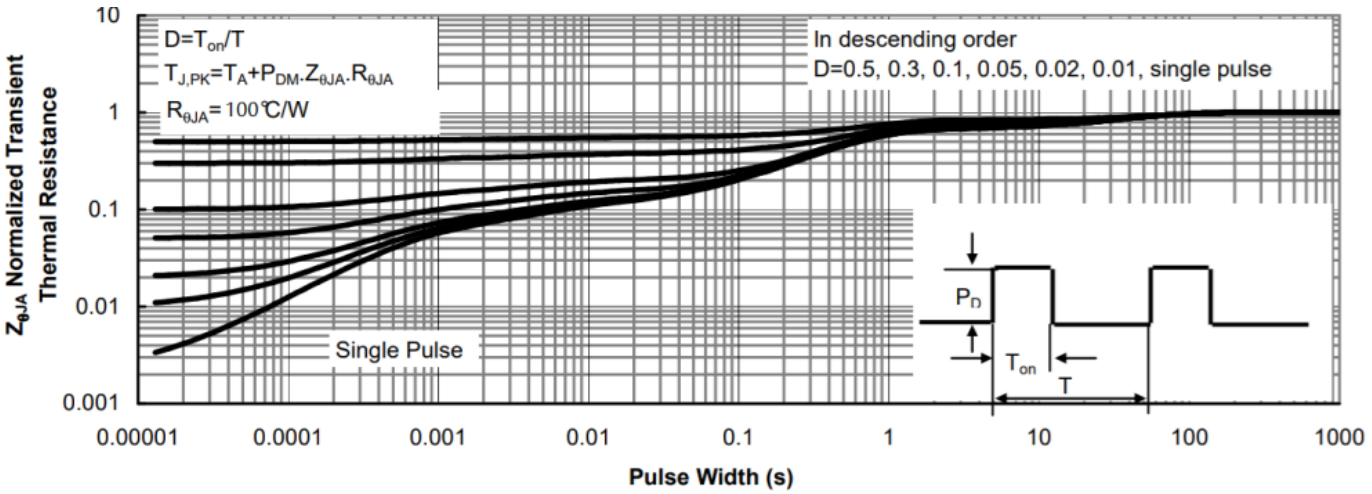
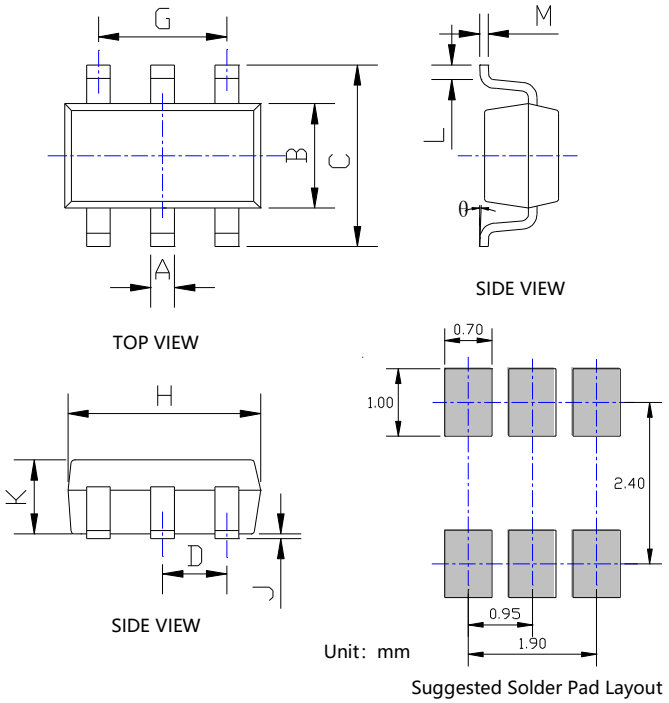


Figure 9. Normalized Maximum Transient Thermal Impedance

■SOT-23-6L Package information



DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.012	0.020	0.300	0.500
B	0.059	0.067	1.500	1.700
C	0.104	0.116	2.650	2.950
D	0.037BSC		0.950BSC	
G	0.075BSC		1.900BSC	
H	0.111	0.119	2.820	3.020
J	0.000	0.004	0.000	0.100
K	0.041	0.045	1.050	1.150
L	0.012	0.024	0.300	0.600
M	0.004	0.008	0.100	0.200
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

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