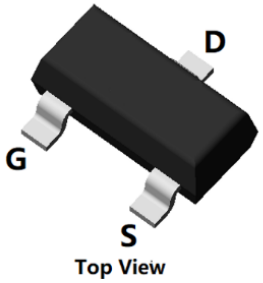
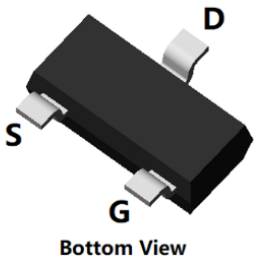
P-Channel Enhancement Mode Field Effect Transistor

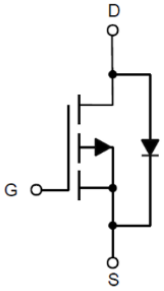


Top View



Bottom View

SOT-23



Product Summary

- V_{DS} -20V
- I_D -5.4A
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜39mohm
- $R_{DS(ON)}$(at V_{GS}=-2.5V) ＜49mohm
- $R_{DS(ON)}$(at V_{GS}=-1.8V) ＜63mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High Power and Current handing capability
- Moisture Sensitivity Level 1
- Low Gate Charge

Applications

- Battery protection
- Power management
- Load switch

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	±10	V
Drain Current	T_A=25℃	I_D	-5.4	A
	T_A=70℃		-4.4	
Pulsed Drain Current [A]		I_{DM}	-22	A
Total Power Dissipation	T_A=25℃	P_D	1.2	W
	T_A=70℃		0.8	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	104	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
L2305B	F2	$S5_B$.	3000	30000	120000	7“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-5.4A		27	39	mΩ
		V_{GS}=-2.5V, I_D=-4A		36	49	
		V_{GS}=-1.8V, I_D=-3A		48	63	
Diode Forward Voltage	V_{SD}	I_S=-5.4A,V_{GS}=0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHz		1010		pF
Output Capacitance	C_{oss}			130		
Reverse Transfer Capacitance	C_{rss}			109		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-4.5V,V_{DS}=-10V,I_D=-4A		10.98		nC
Gate-Source Charge	Q_{gs}			2.17		
Gate-Drain Charge	Q_{gd}			2.54		
Reverse Recovery Chrage	Q_{rr}	I_F=-4A, di/dt=100A/us		4.38		
Reverse Recovery Time	t_{rr}			25		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V, V_{DS}=-10V, R_L=2.5Ω R_{GEN}=3Ω		8		
Turn-on Rise Time	t_r			36		
Turn-off Delay Time	$t_{D(off)}$			77		
Turn-off fall Time	t_f			56		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

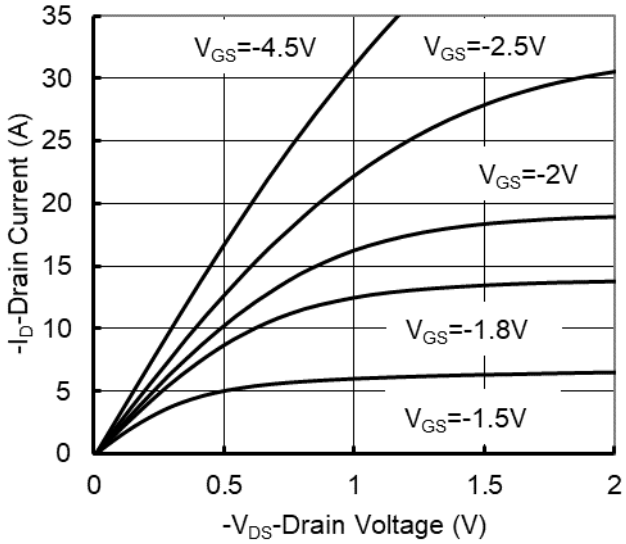


Figure1. Output Characteristics

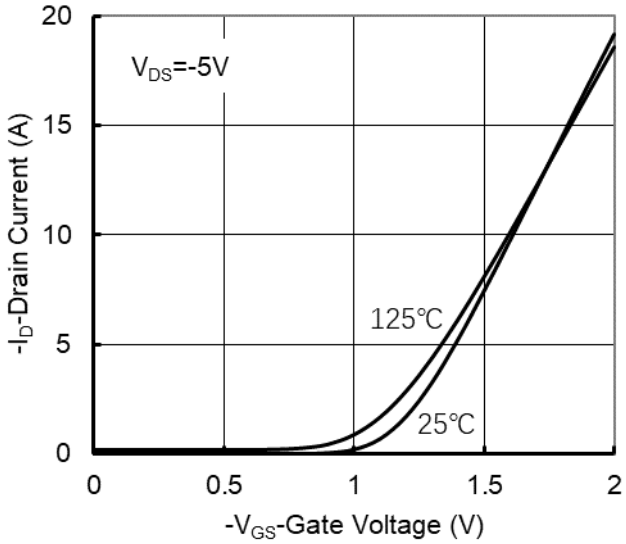


Figure2. Transfer Characteristics

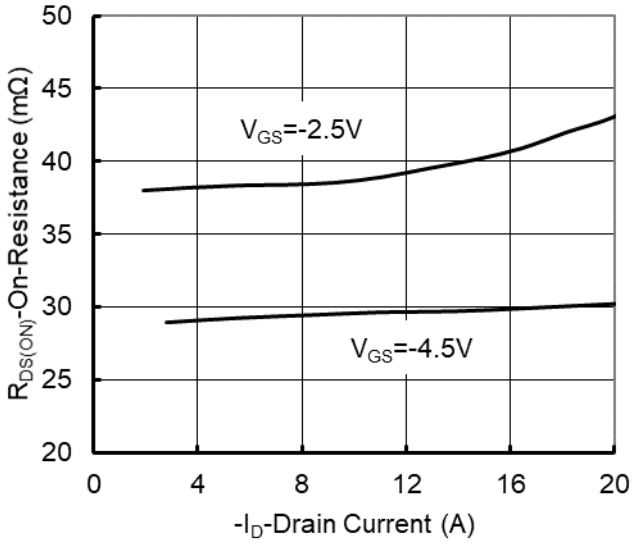


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

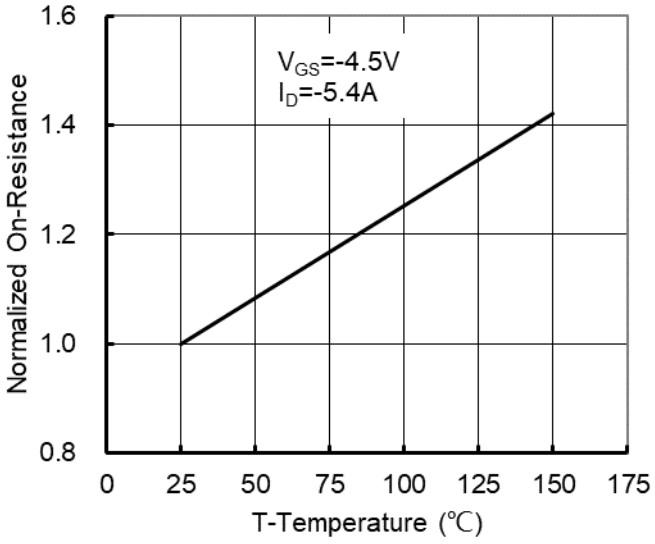


Figure 4: On-Resistance vs. Junction Temperature

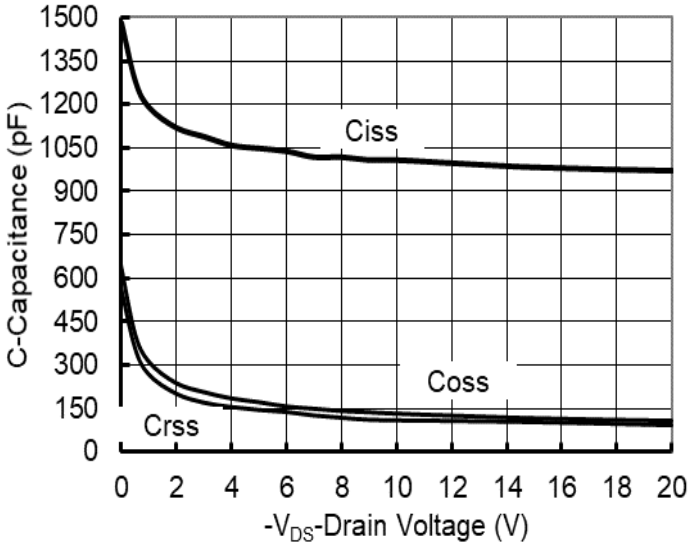


Figure5. Capacitance Characteristics

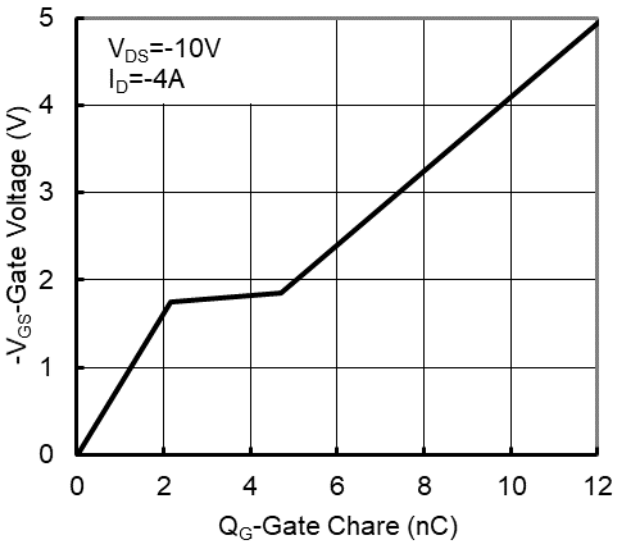


Figure6. Gate Charge

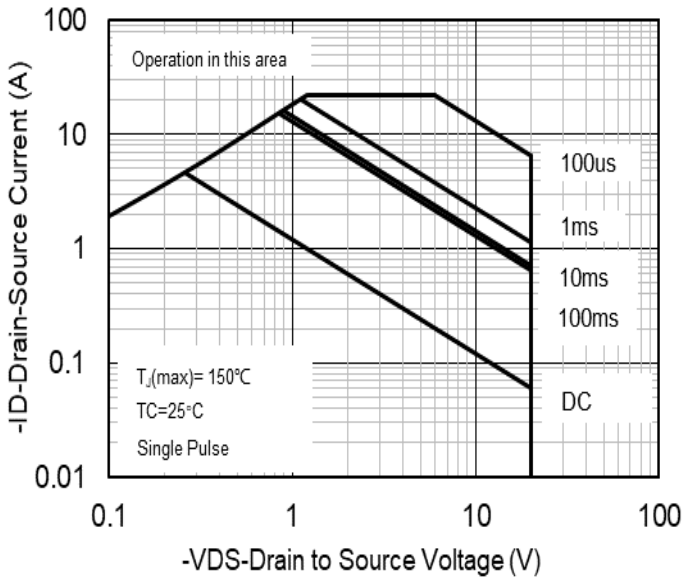


Figure7. Safe Operation Area

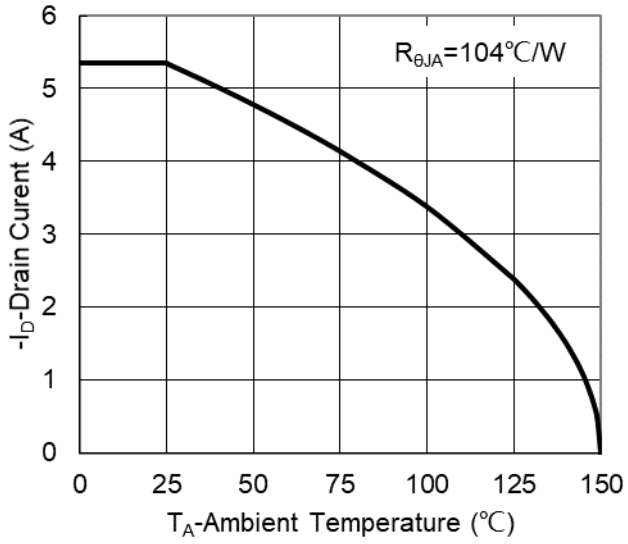


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

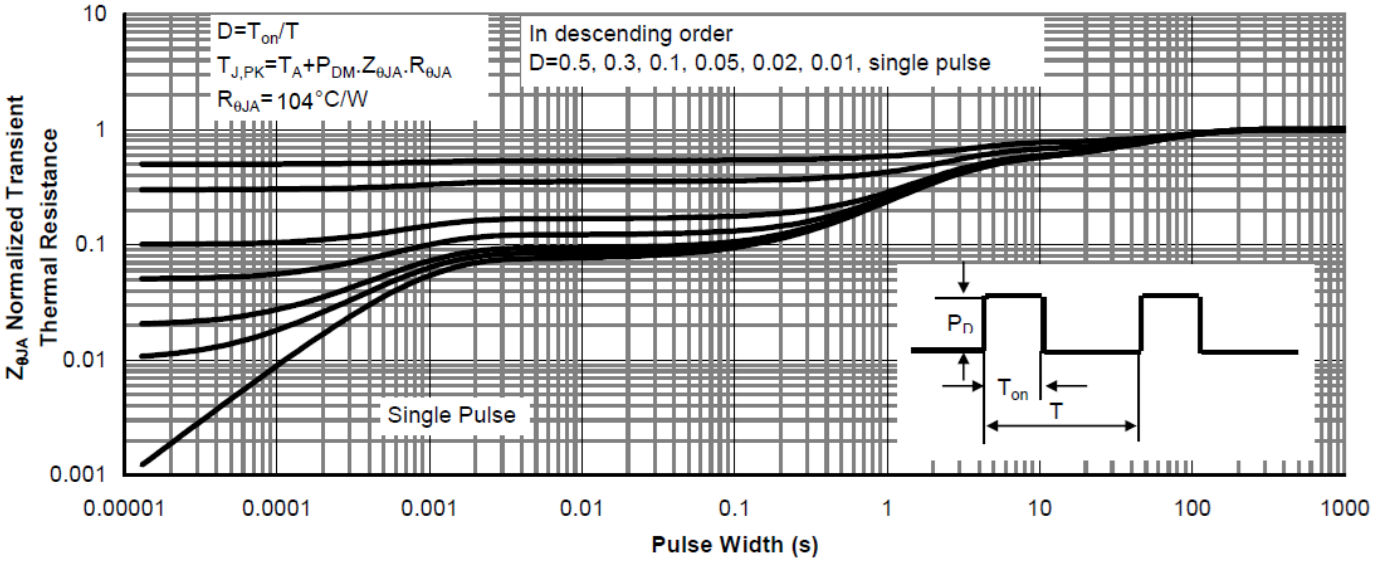
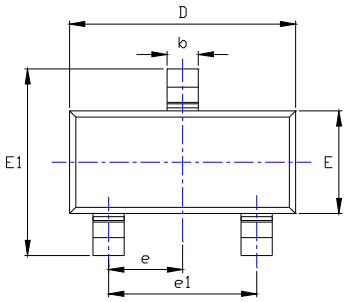
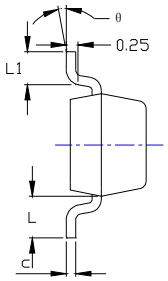


Figure9. Normalized Maximum Transient Thermal Impedance

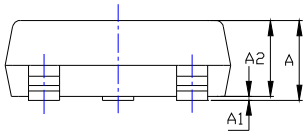
■ SOT-23 Package Information



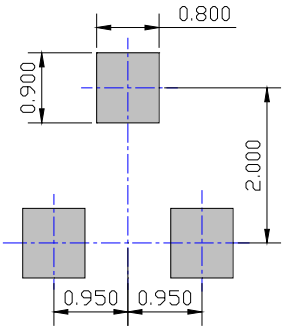
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.200	0.300	0.500
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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