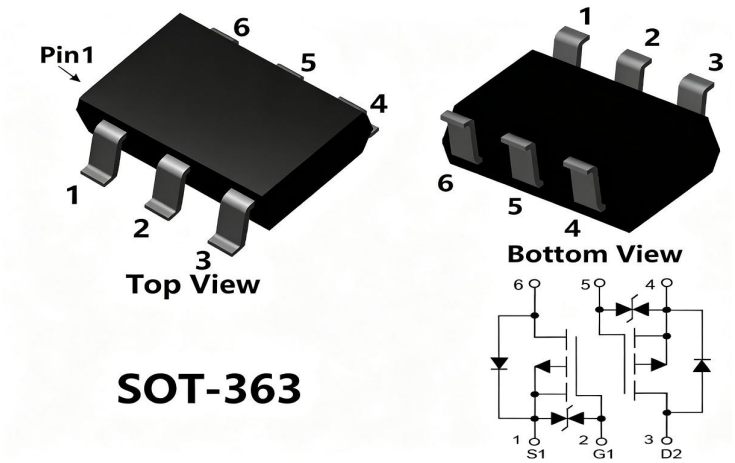
P-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} -20V
- I_D -0.5A
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜850 mohm
- $R_{DS(ON)}$(at V_{GS}=-2.5V) ＜1200 mohm
- $R_{DS(ON)}$(at V_{GS}=-1.8V) ＜2000 mohm
- ESD Protected Up to 2.0KV (HBM)

General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Interfacing, Logic switch
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	±12	V
Drain Current	T_A=25℃ Steady State	I_D	-0.5	A
	T_A=70℃ Steady State		-0.4	
Pulsed Drain Current [A]		I_{DM}	-2.6	A
Total Power Dissipation @ T_A=25℃ Steady State		P_D	0.15	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]		$R_{\theta JA}$	833	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
L3139KADW	F2	39KA	3000	30000	120000	7“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±10V, V_{DS}=0V		±1.5	±10	μA
		V_{GS}= ±8V, V_{DS}=0V		±500	±2000	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-0.35	-0.62	-1.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -4.5V, I_D=-0.5A		580	850	mΩ
		V_{GS}= -2.5V, I_D=-0.3A		855	1200	
		V_{GS}= -1.8V, I_D=-0.2A		1350	2000	
Diode Forward Voltage	V_{SD}	I_S=-0.5A,V_{GS}=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-0.5	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHZ		71		pF
Output Capacitance	C_{oss}			20		
Reverse Transfer Capacitance	C_{rss}			15		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-4.5V,V_{DD}=-10V,I_D=-0.5A		1.24		nC
Gate Source Charge	Q_{gs}			0.37		
Gate Drain Charge	Q_{gd}			0.27		
Reverse Recovery Chrage	Q_{rr}	I_F=-0.5A, di/dt=-20A/us		0.97		
Reverse Recovery Time	t_{rr}			26		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V,V_{DD}=-10V, R_L=2.5Ω, R_{GEN}=3Ω		4		
Turn-on Rise Time	t_r			19		
Turn-off Delay Time	$t_{D(off)}$			16		
Turn-off Fall Time	t_f			25		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

■ Typical Performance Characteristics

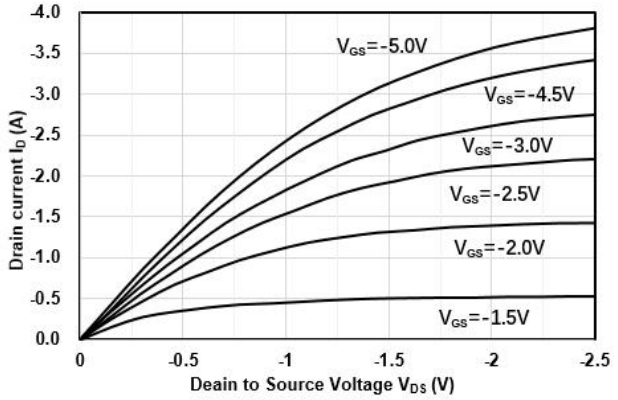


Figure1. Output Characteristics

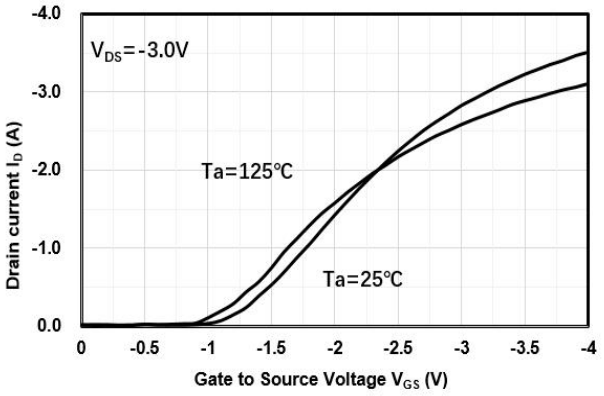


Figure2. Transfer Characteristics

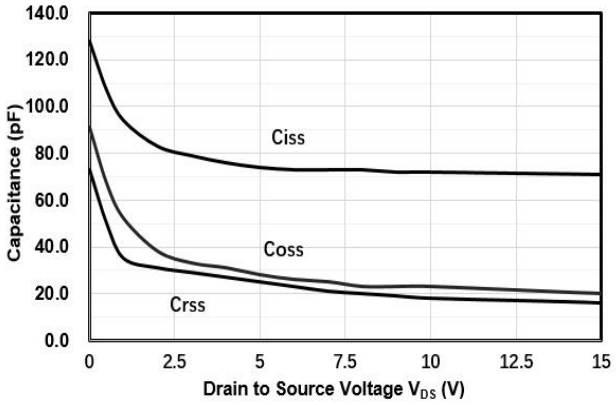


Figure3. Capacitance Characteristics

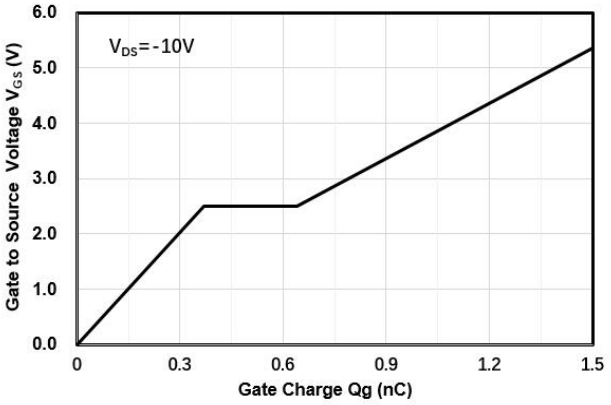


Figure4. Gate Charge

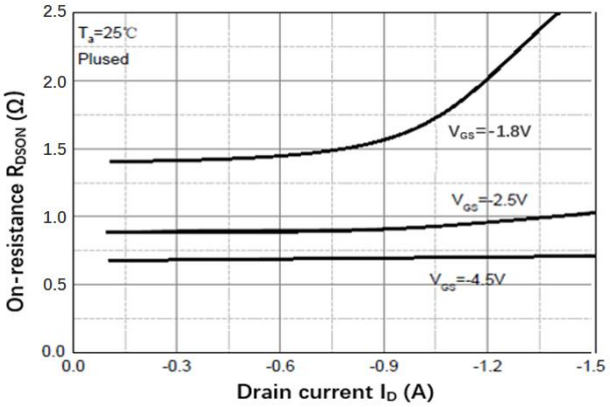


Figure5. Drain-Source on Resistance

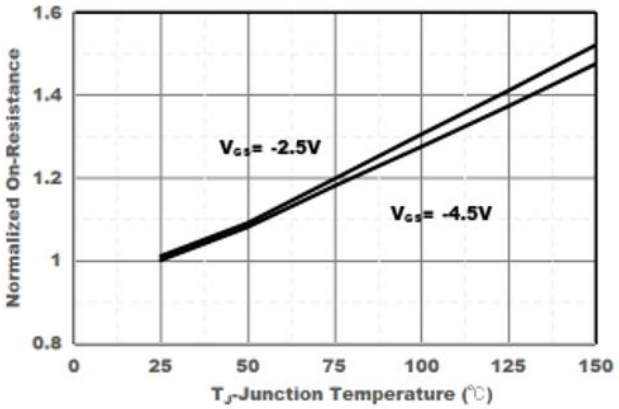


Figure6. Drain-Source on Resistance

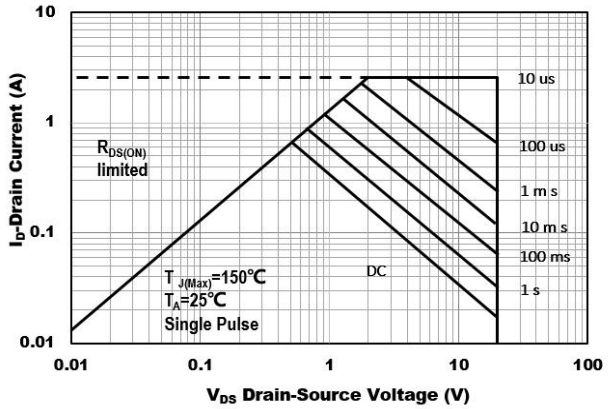


Figure7. Safe Operation Area

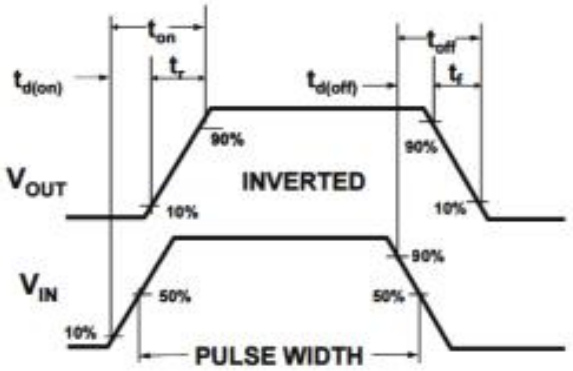
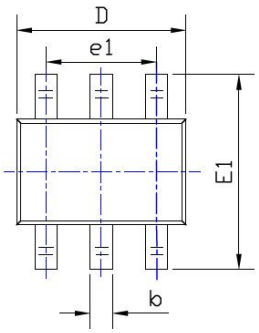
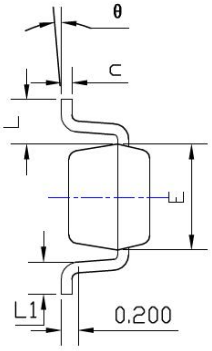


Figure8. Switching wave

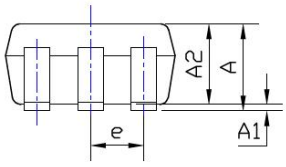
■ SOT-363 Package information



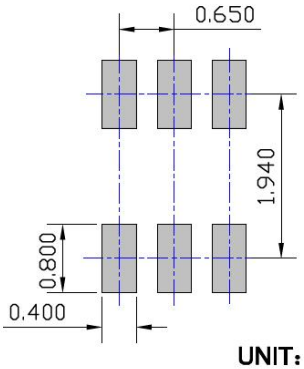
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.043	0.900	1.100
A1	0.000	0.004	0.000	0.100
A2	0.035	0.039	0.900	1.000
b	0.006	0.014	0.150	0.350
c	0.004	0.010	0.100	0.250
D	0.071	0.087	1.800	2.200
E	0.045	0.053	1.150	1.350
E1	0.085	0.096	2.150	2.450
e	0.026TYP		0.650TYP	
e1	0.047	0.055	1.200	1.400
L	0.021REF		0.525REF	
L1	0.010	0.018	0.260	0.460
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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