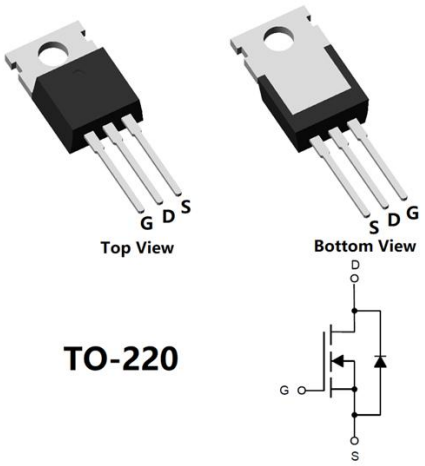
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 73A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜8mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- PD

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	100	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	13.8	A
		T_A=100℃,V_{GS}=10V		-	8.7	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V,Chip limitation		-	73	
		T_C=100℃,V_{GS}=10V		-	46	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	292	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		68	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=21.7A		EAS	-	117.7	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	2.9	W
		T_A=100℃		-	1.16	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	81.6	
		T_C=100℃		-	32.6	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	150	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	43	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	1.53	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
P8D0G10H	B1	P8D0G10H	50	/	5000	Tube

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=1mA,Tj=25℃	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=80V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2.2	2.8	3.7	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=50A,Tj=25℃	-	6.1	8	mΩ
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V,Tj=25℃	-	0.92	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	1.5	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=100KHz,Tj=25℃	-	1404	-	pF
Output Capacitance	C_{oss}		-	681	-	
Reverse Transfer Capacitance	C_{rss}		-	21	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=50A,Tj=25℃	-	23.7	-	nC
Gate-Source Charge	Q_{gs}		-	7.5	-	
Gate-Drain Charge	Q_{gd}		-	6.8	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs,V_{GS}=0V,V_R=50V,Tj=25℃	-	20.7	-	nC
Reverse Recovery Time	t_{rr}		-	30.7	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=50V,I_D=50A,R_{GEN}=6.2Ω, Tj=25℃	-	13.1	-	ns
Turn-on Rise Time	t_r		-	51.5	-	
Turn-off Delay Time	$t_{D(off)}$		-	24.4	-	
Turn-off Fall Time	t_f		-	13.7	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

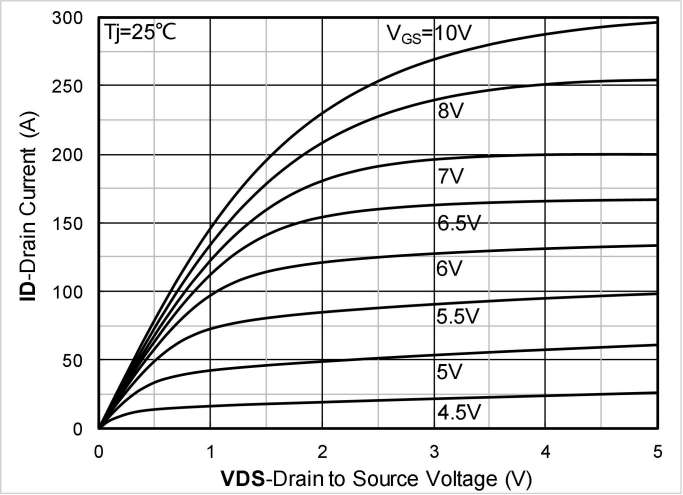


Figure 1. Output Characteristics; typical values

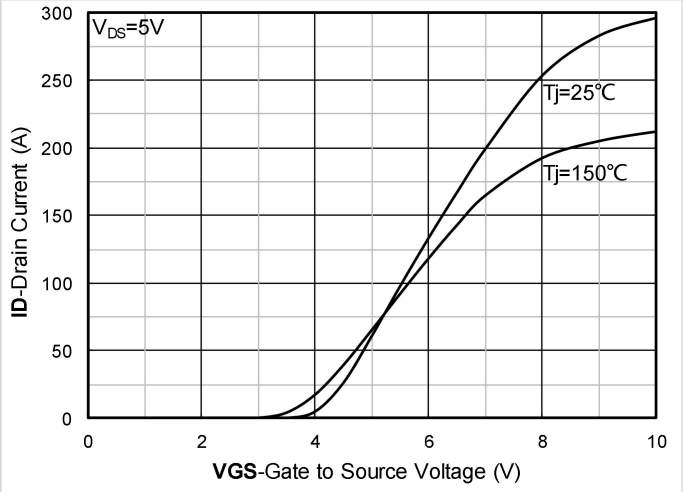


Figure 2. Transfer Characteristics; typical values

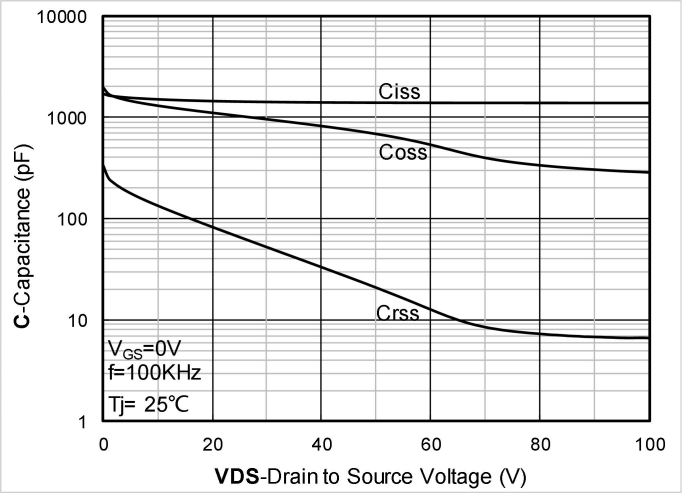


Figure 3. Capacitance Characteristics; typical values

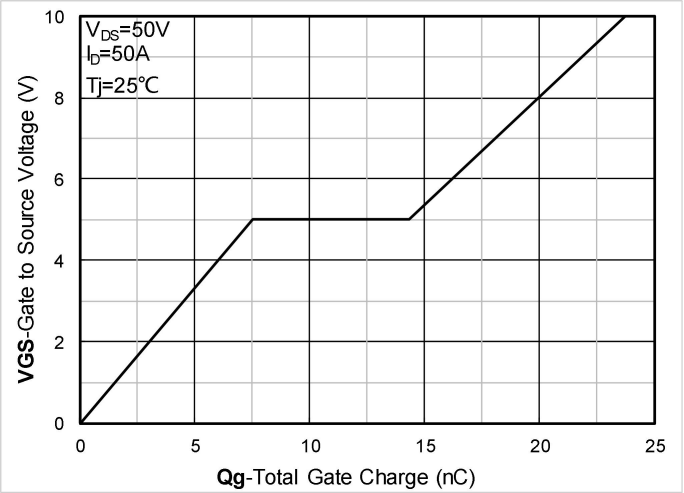


Figure 4. Gate Charge; typical values

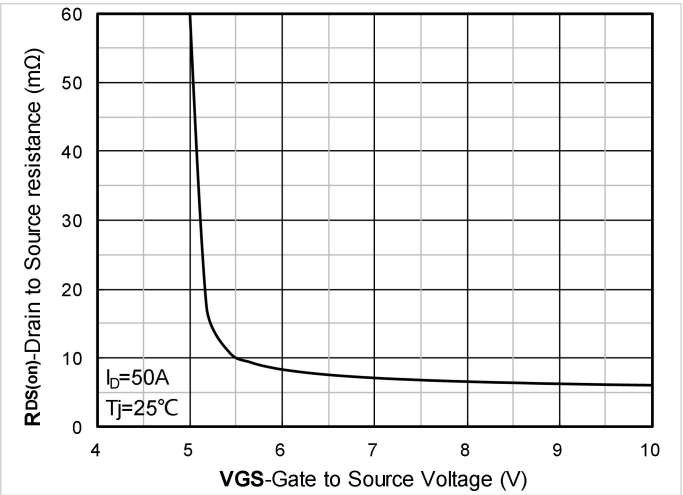


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

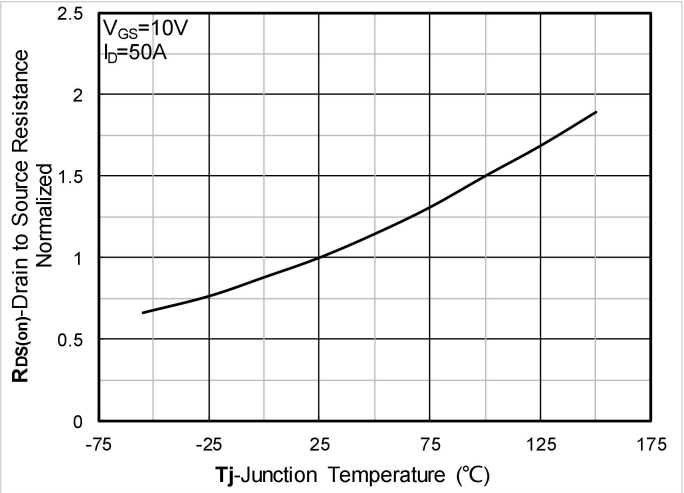


Figure 6. Normalized On-Resistance

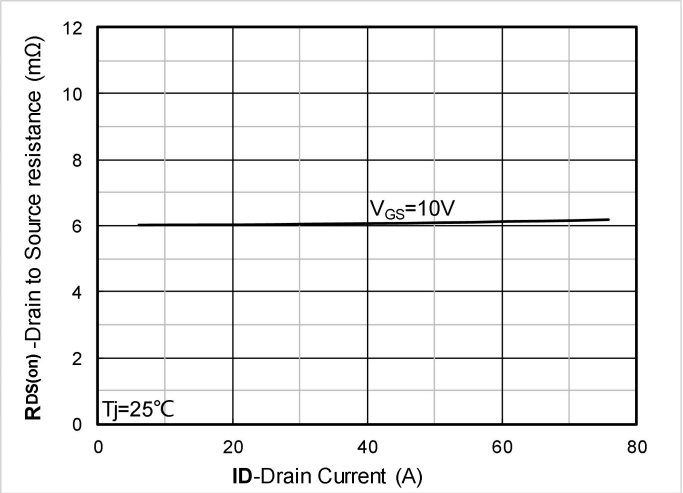


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

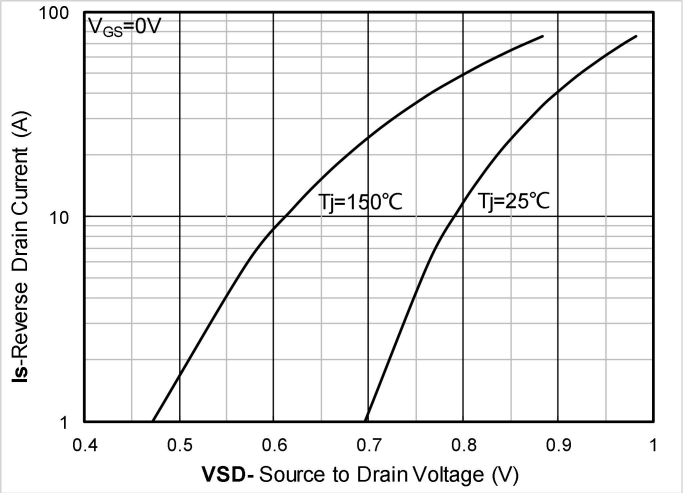


Figure 8. Forward characteristics of reverse diode; typical values

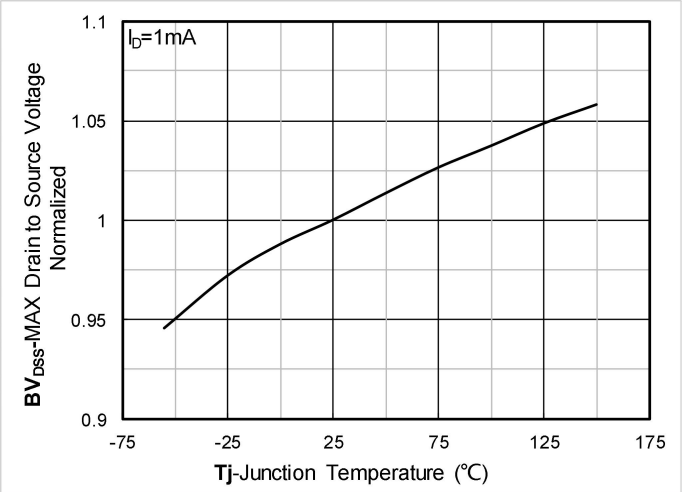


Figure 9. Normalized breakdown voltage

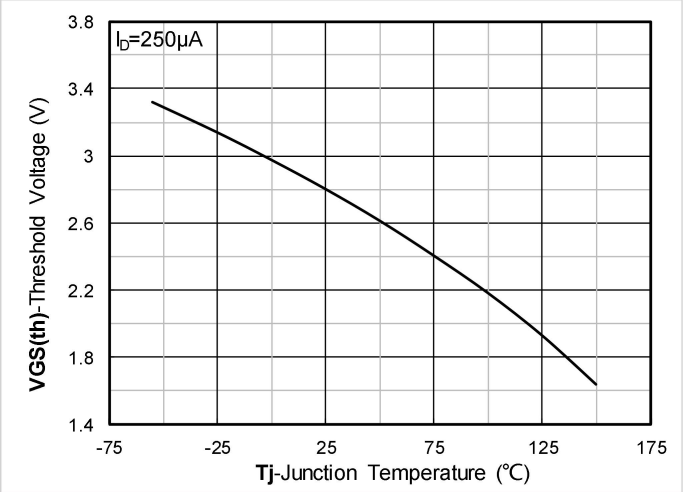


Figure 10. Gate Threshold voltage; typical values

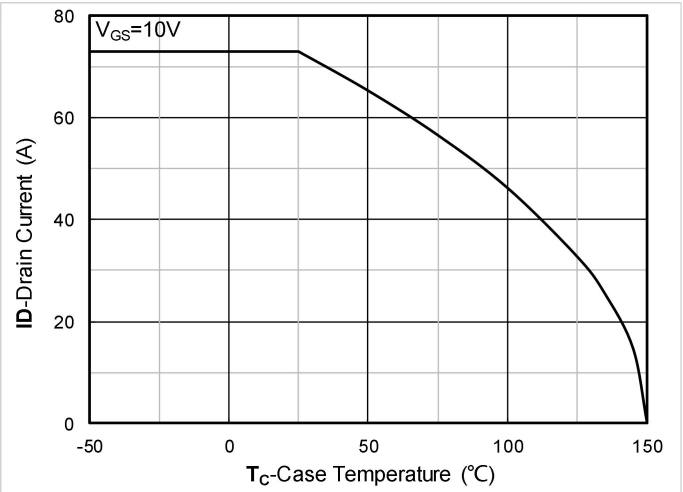


Figure 11. Current dissipation

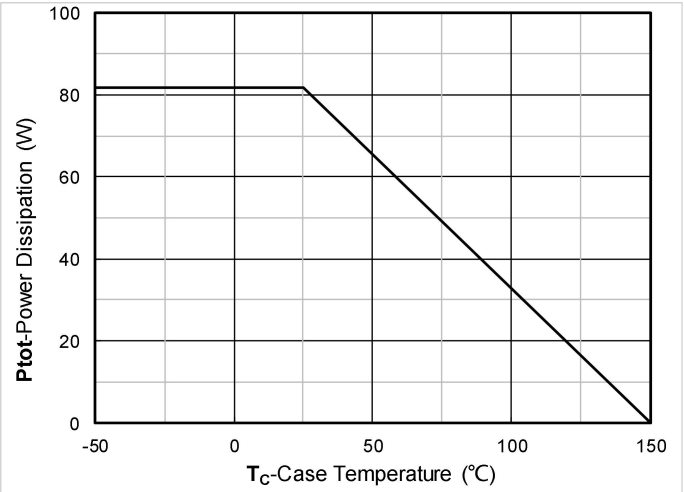


Figure 12. Power dissipation

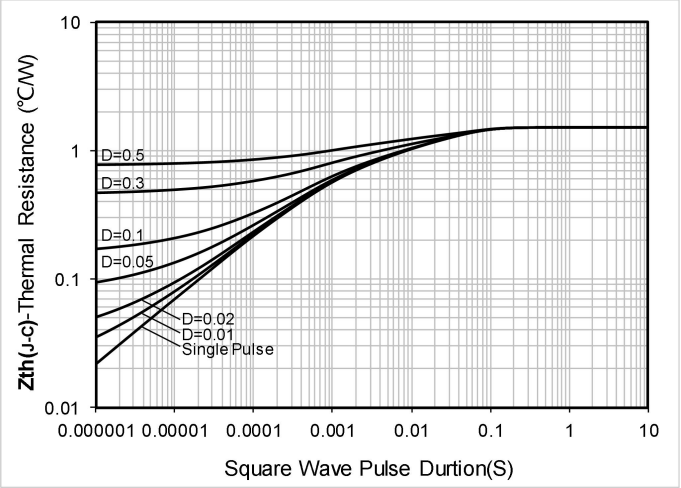


Figure 13. Maximum Transient Thermal Impedance

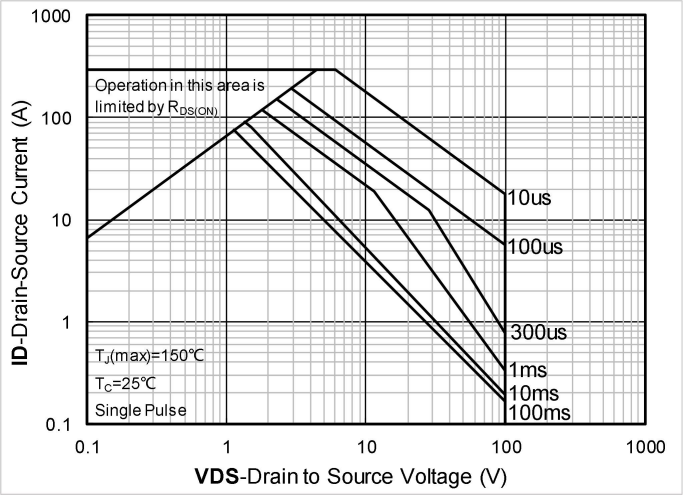
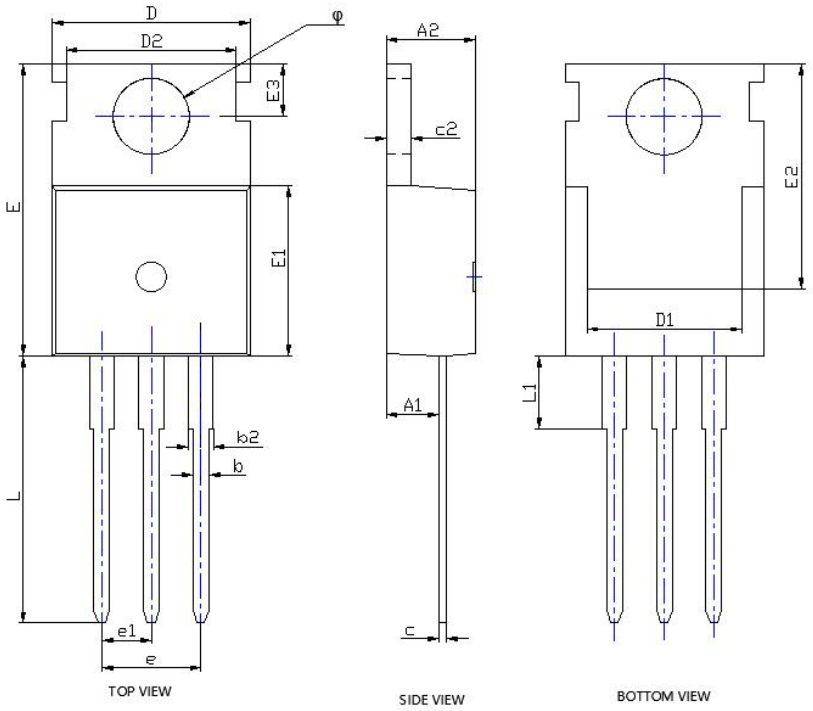


Figure 14. Safe Operation Area

■ TO-220AB-C Package information



DIMENSIONS				
SYMBOL	INCHES		Millmeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.091	0.098	2.300	2.500
A2	0.173	0.181	4.400	4.600
b	0.028	0.035	0.700	0.900
b2	0.049	0.056	1.250	1.420
c	0.018	0.022	0.450	0.550
c2	0.049	0.053	1.250	1.350
D	0.382	0.402	9.700	10.200
D1	0.295	0.331	7.500	8.400
D2	0.335	0.350	8.500	8.900
E	0.602	0.634	15.300	16.100
E1	0.358	0.366	9.100	9.300
E2	0.497	0.525	12.630	13.330
E3	0.108BSC		2.750BSC	
e	0.200BSC		5.080BSC	
e1	0.100BSC		2.540BSC	
L	0.512	0.531	13.000	13.500
L1	---	0.138	---	3.500
ø	0.140	0.148	3.550	3.750

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.

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