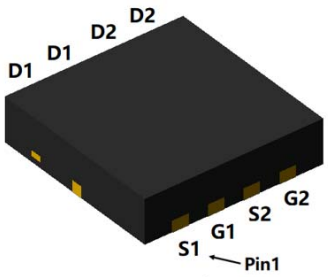
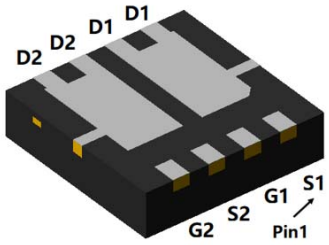
# N-Channel and P-Channel Complementary MOSFET

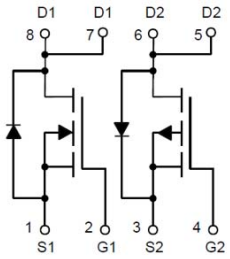



Top View




Bottom View

DFN3333-8L




## Product Summary

**NMOS**

- $V_{DS}$ 30V
- $I_D$ 20A
- $R_{DS(ON)}$( at $V_{GS}$=10V) ＜20mΩ
- $R_{DS(ON)}$( at $V_{GS}$=4.5V) ＜30mΩ

**PMOS**

- $V_{DS}$ -30V
- $I_D$ -20A
- $R_{DS(ON)}$( at $V_{GS}$=-10V) ＜18mΩ
- $R_{DS(ON)}$( at $V_{GS}$=-4.5V) ＜25mΩ
- 100% EAS Tested

## General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

## Applications

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

## ■ Absolute Maximum Ratings ($T_A$=25℃ unless otherwise noted)

| Parameter | | Symbol | NMOS | PMOS | Unit |
|---|---|---|---|---|---|
| Drain-source Voltage | | $V_{DS}$ | 30 | -30 | V |
| Gate-source Voltage | | $V_{GS}$ | ±20 | ±20 | V |
| Drain Current | $T_A$=25℃ | $I_D$ | 6.5 | 7.5 | A |
| | $T_A$=100℃ | | 4 | 4.7 | |
| | $T_C$=25℃ | | 20 | -20 | |
| | $T_C$ =100℃ | | 12 | -12 | |
| Pulsed Drain Current [A] | | $I_{DM}$ | 60 | -80 | A |
| Avalanche energy [B] | | EAS | 25 | 81 | mJ |
| Total Power Dissipation [C] | $T_A$=25℃ | $P_D$ | 2 | 2 | W |
| | $T_A$=100℃ | | 0.8 | 0.8 | |
| | $T_C$=25℃ | | 27 | 22 | |
| | $T_C$ =100℃ | | 11 | 9 | |
| Junction and Storage Temperature Range | | $T_J$ ,$T_{STG}$ | -55～+150 | -55～+150 | ℃ |

## ■Thermal resistance

| Parameter | | Symbol | NMOS | | PMOS | | Units |
|---|---|---|---|---|---|---|---|
| | | | Typ | Max | Typ | Max | |
| Thermal Resistance Junction-to-Ambient [D] | Steady-State | $R_{\theta JA}$ | 50 | 62.5 | 50 | 62.5 | ℃/W |
| Thermal Resistance Junction-to-Case | Steady-State | $R_{\theta JC}$ | 3.5 | 4.5 | 4.5 | 5.5 | |

## ■ Ordering Information (Example)

| PREFERED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---|---|---|---|---|---|---|
| Q20NP03A | F1 | Q20NP03A | 5000 | 10000 | 100000 | 13'' reel |

## ■ NMOS Electrical Characteristics ($T_J$=25℃ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$= 0V, $I_D$=250μA | 30 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=30V, $V_{GS}$=0V | - | - | 1 | μA |
| | | $V_{DS}$=30V, $V_{GS}$=0V, Tj=150℃ | - | - | 100 | |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$= ±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$= $V_{GS}$, $I_D$=250μA | 1.0 | 1.5 | 2.5 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$=10V, $I_D$=20A | - | 14 | 20 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=10A | - | 22 | 30 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=20A, $V_{GS}$=0V | - | 0.85 | 1.2 | V |
| Gate resistance | $R_G$ | f=1MHz | - | 2 | - | Ω |
| Maximum Body-Diode Continuous Current | $I_S$ | | - | - | 20 | A |
| **Dynamic Parameters** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=15V, $V_{GS}$=0V, f=1MHz | - | 380 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 75 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 60 | - | |
| **Switching Parameters** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=10A | - | 12.5 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 2.8 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 2.5 | - | |
| Reverse Recovery Charge | $Q_{rr}$ | $I_F$=10A, di/dt=350A/us | - | 1.7 | - | nC |
| Reverse Recovery Time | $t_{rr}$ | | - | 18 | - | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}$=10V, $V_{DD}$=15V, $I_D$=10A $R_{GEN}$=3Ω | - | 5 | - | ns |
| Turn-on Rise Time | $t_r$ | | - | 31 | - | |
| Turn-off Delay Time | $t_{D(off)}$ | | - | 15 | - | |
| Turn-off fall Time | $t_f$ | | - | 23 | - | |

## ■ PMOS Electrical Characteristics ($T_J$=25℃ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$= 0V, $I_D$=-250μA | -30 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-30V, $V_{GS}$=0V | - | - | -1 | μA |
| | | $V_{DS}$=-30V, $V_{GS}$=0V, Tj=150℃ | - | - | -100 | |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$= ±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$= $V_{GS}$, $I_D$=-250μA | -1.0 | -1.5 | -2.5 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS}$=-10V, $I_D$=-20A | - | 13.5 | 18 | mΩ |
| | | $V_{GS}$=-4.5V, $I_D$=-10A | - | 19 | 25 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=-20A, $V_{GS}$=0V | - | -0.85 | -1.2 | V |
| Gate resistance | $R_G$ | f=1MHz | - | 15 | - | Ω |
| Maximum Body-Diode Continuous Current | $I_S$ | | - | - | -20 | A |
| **Dynamic Parameters** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=-15V, $V_{GS}$=0V, f=1MHz | - | 1220 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 170 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 160 | - | |
| **Switching Parameters** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$=-10V, $V_{DS}$=-15V, $I_D$=-10A | - | 24 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 2 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 6 | - | |
| Reverse Recovery Charge | $Q_{rr}$ | $I_F$=-10A, di/dt=100A/us | - | 11 | - | nC |
| Reverse Recovery Time | $t_{rr}$ | | - | 35 | - | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}$=-10V, $V_{DD}$=-15V, ID=-10A $R_{GEN}$=2.5Ω | - | 11 | - | ns |
| Turn-on Rise Time | $t_r$ | | - | 4 | - | |
| Turn-off Delay Time | $t_{D(off)}$ | | - | 70 | - | |
| Turn-off fall Time | $t_f$ | | - | 50 | - | |

A. Repetitive rating; pulse width limited by max. junction temperature.
B. NMOS: $T_J$=25℃, $V_{DD}$=30V, $V_{GS}$=10V, $R_G$=25Ω, L=2mH, IAS=5A.
PMOS: $T_J$=25℃, $V_{DD}$=-30V, $V_{GS}$=-10V, $R_G$=25Ω, L=2mH, IAS=-9A.
C. $P_d$ is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 $in^2$ FR-4 board with 2oz. Copper, in the still air environment with $T_A$ =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

## ■ NMOS Typical Electrical and Thermal Characteristics Diagrams

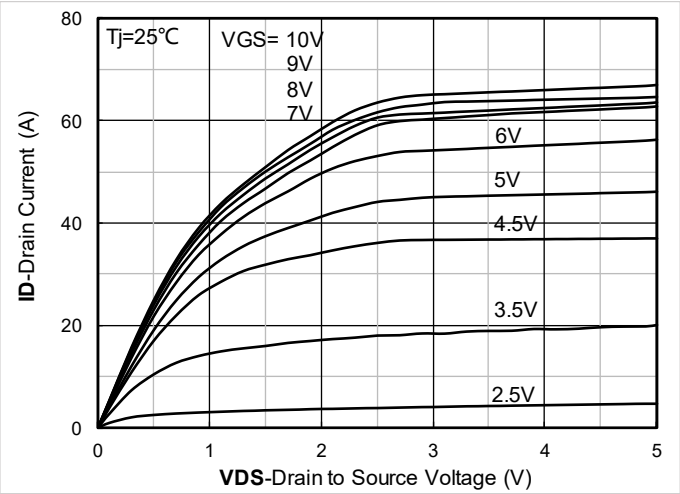



Figure 1. Output Characteristics

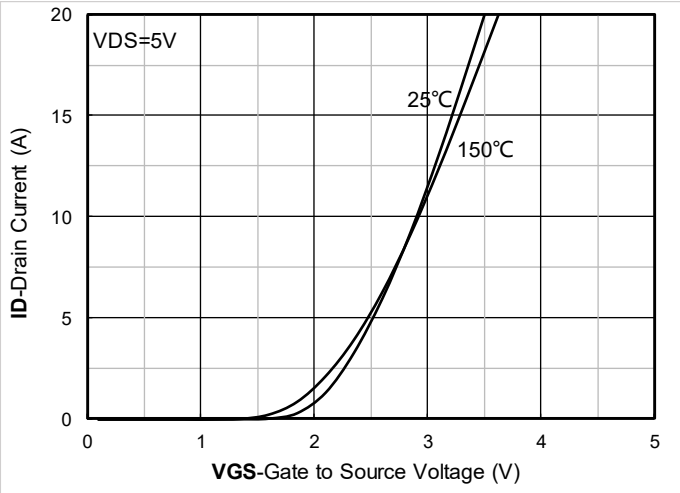



Figure 2. Transfer Characteristics

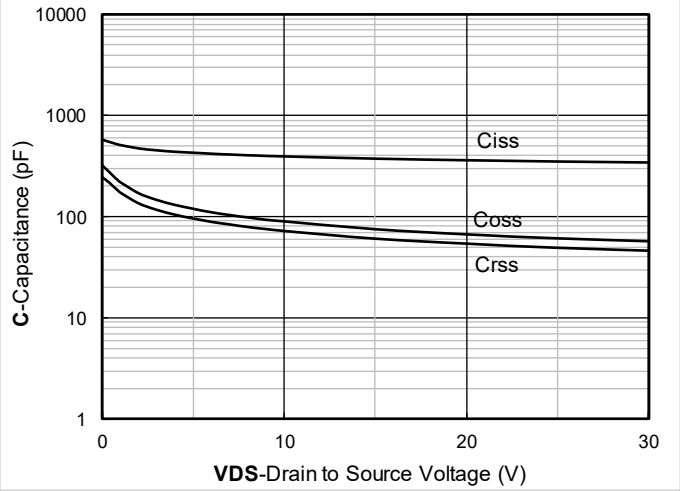



Figure 3. Capacitance Characteristics

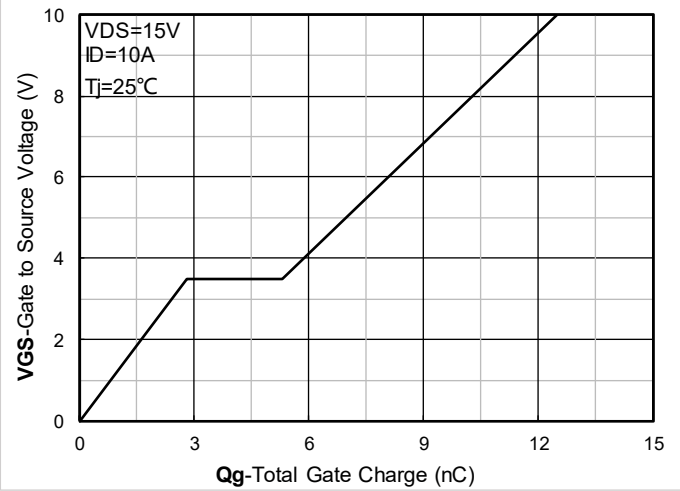



Figure 4. Gate Charge

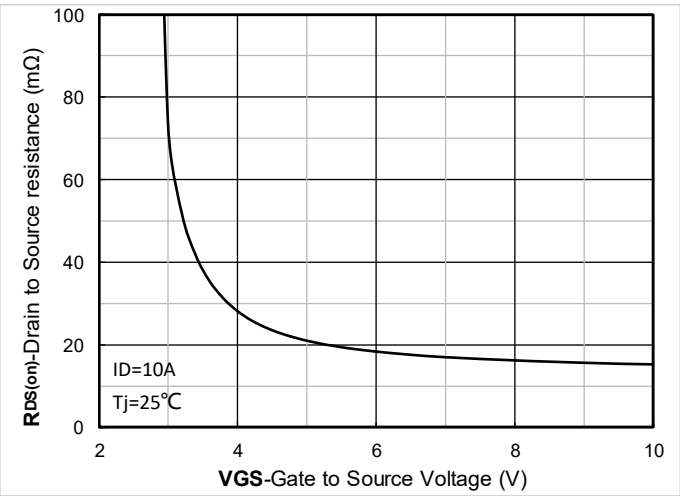



Figure 5. On-Resistance vs Gate to Source Voltage

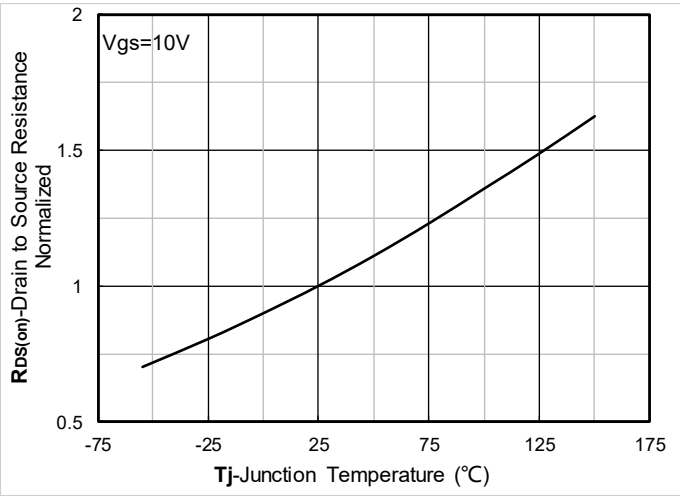



Figure 6. Normalized On- Resistance

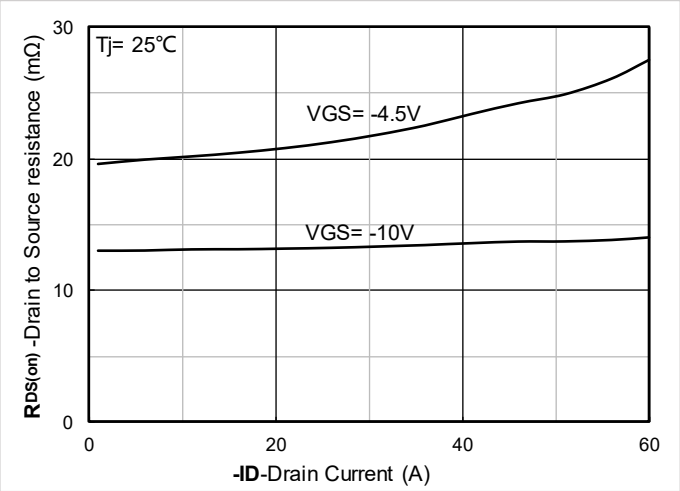



Figure 7. $R_{DS(on)}$ VS Drain Current

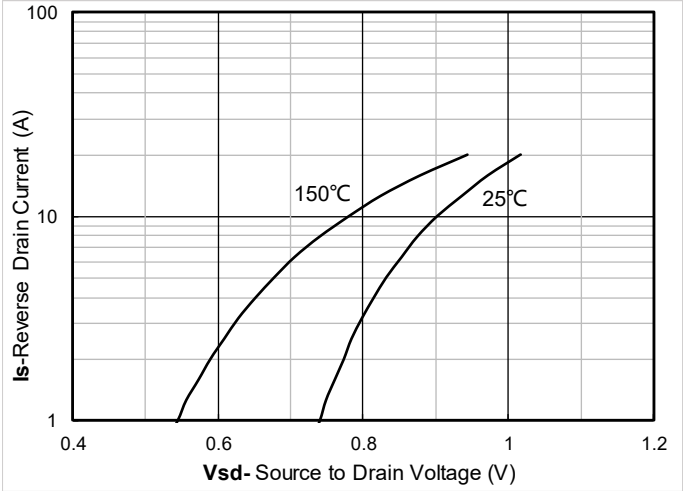



Figure 8. Forward characteristics of reverse diode

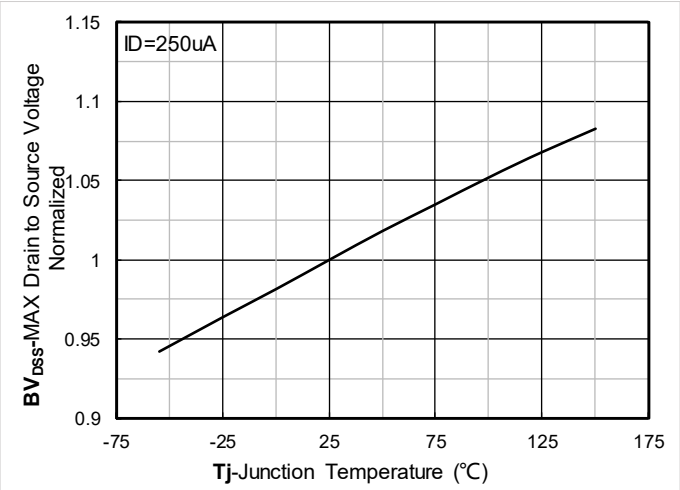



Figure 9. Normalized breakdown voltage

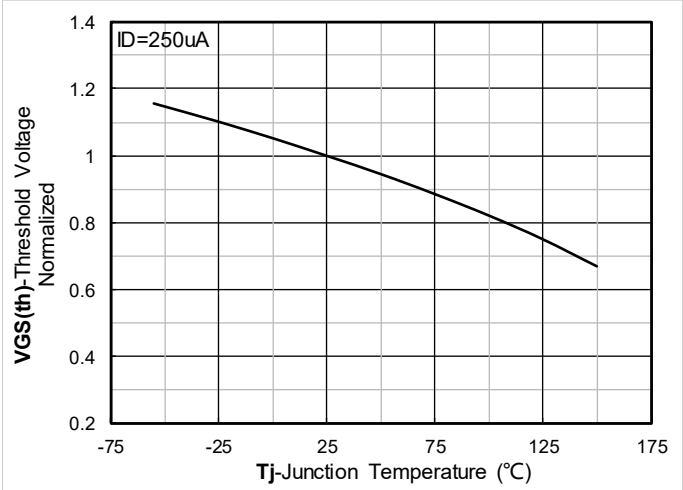



Figure 10. Normalized Threshold voltage

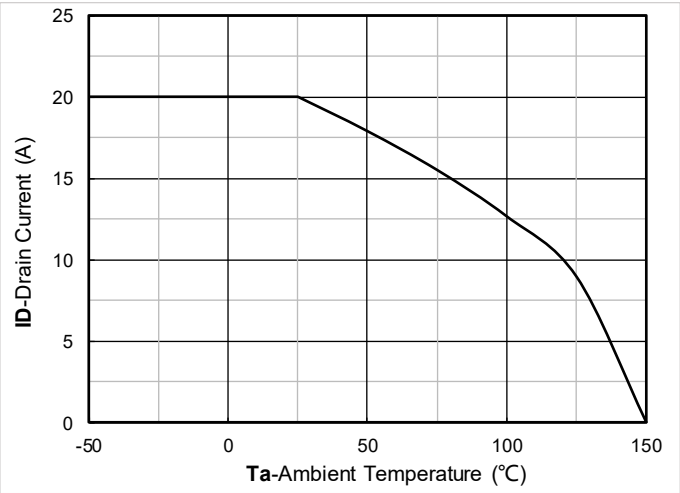



Figure 11. Current dissipation

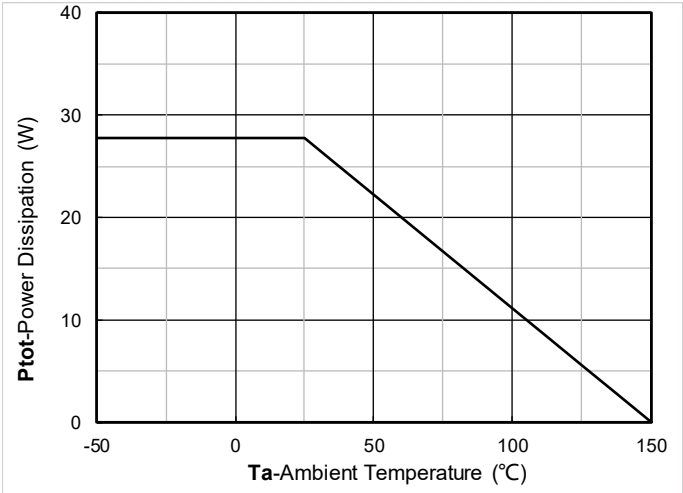



Figure 12. Power dissipation

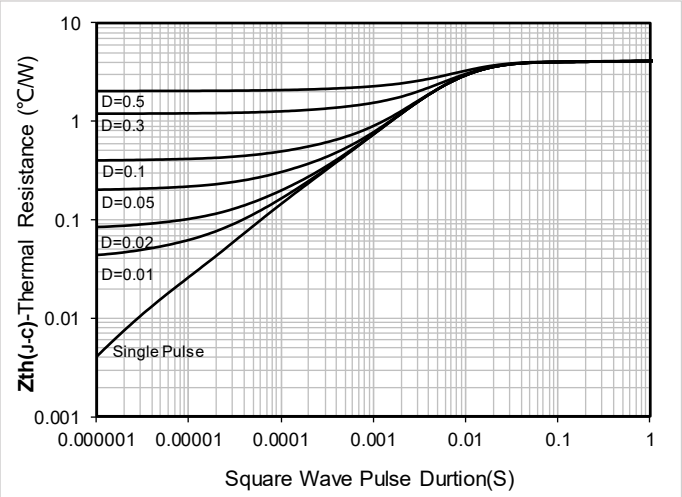



Figure 13. Maximum Transient Thermal Impedance

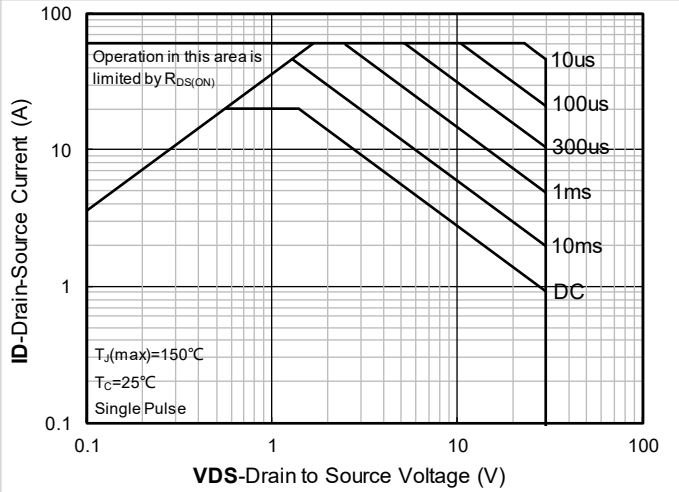



Figure 14. Safe Operation Area

## ■ PMOS Typical Electrical and Thermal Characteristics Diagrams

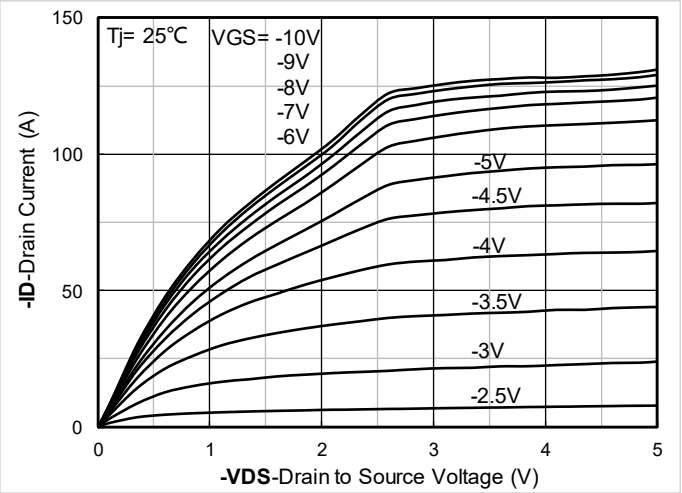



Figure 1. Output Characteristics

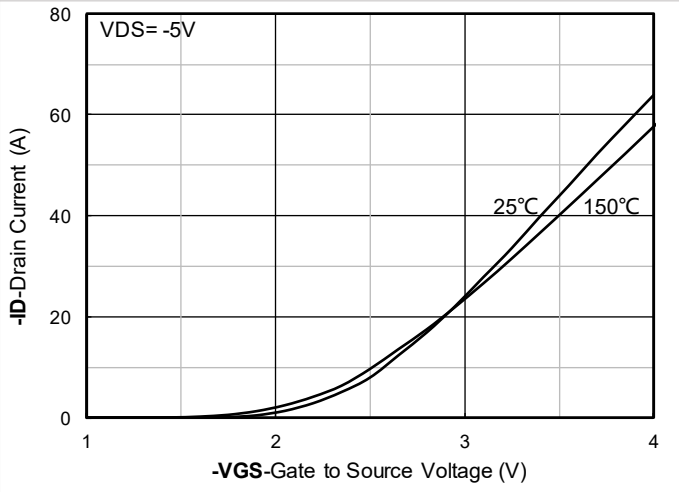



Figure 2. Transfer Characteristics

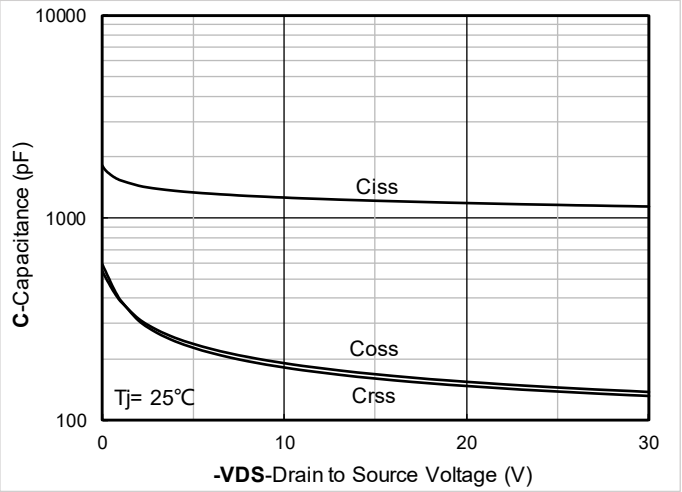



Figure 3. Capacitance Characteristics

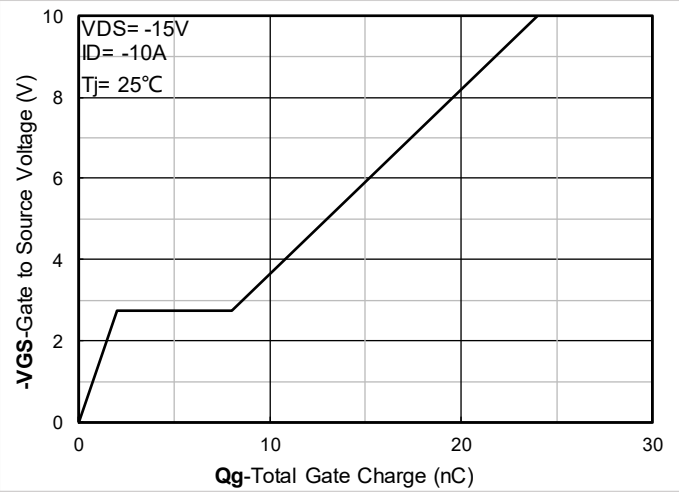



Figure 4. Gate Charge

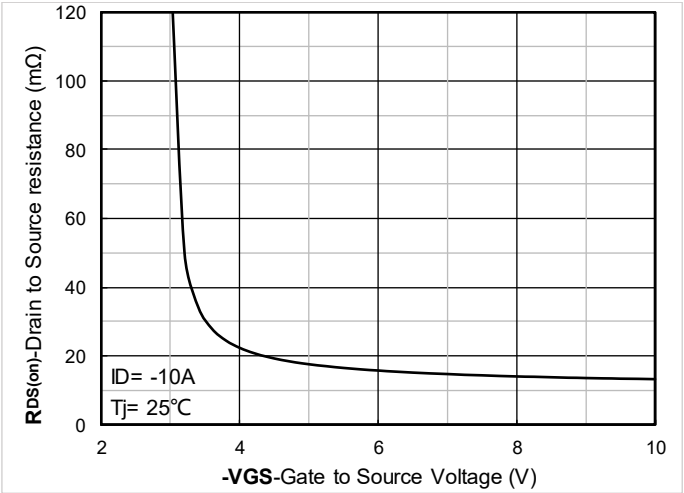



Figure 5. On-Resistance vs Gate to Source Voltage

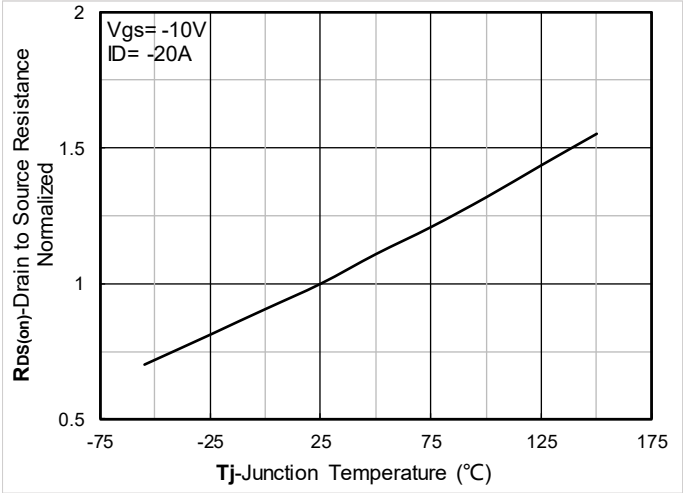



Figure 6. Normalized On-Resistance

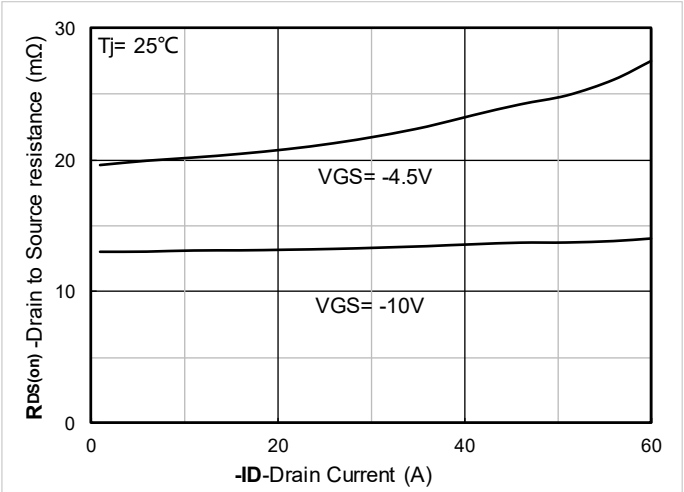



Figure 7. $R_{DS(on)}$ VS Drain Current

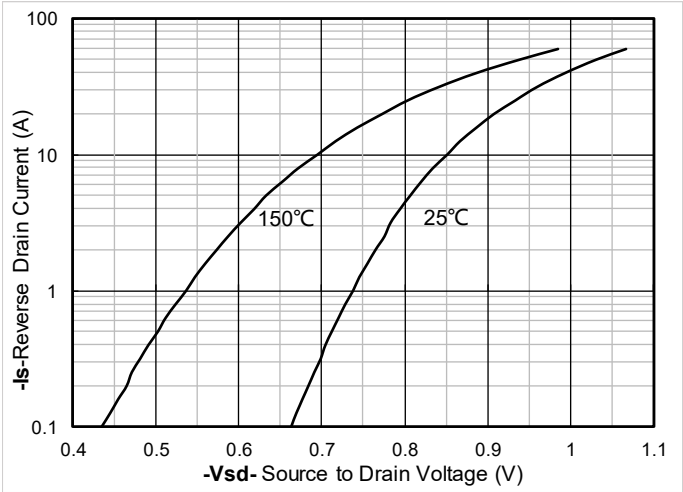



Figure 8. Forward characteristics of reverse diode

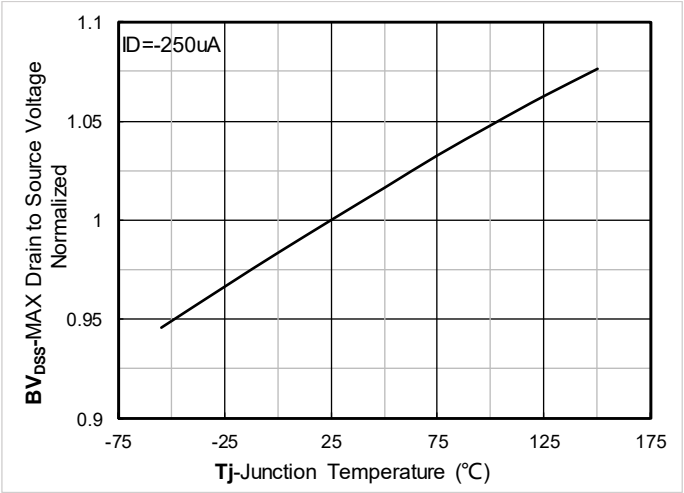



Figure 9. Normalized breakdown voltage

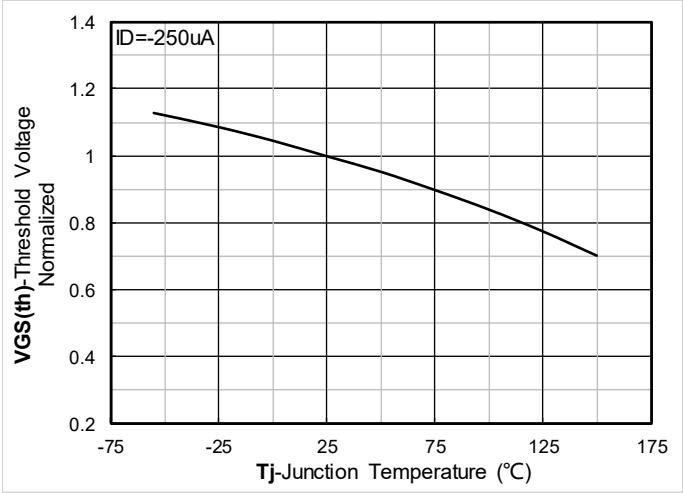



Figure 10. Normalized Threshold voltage

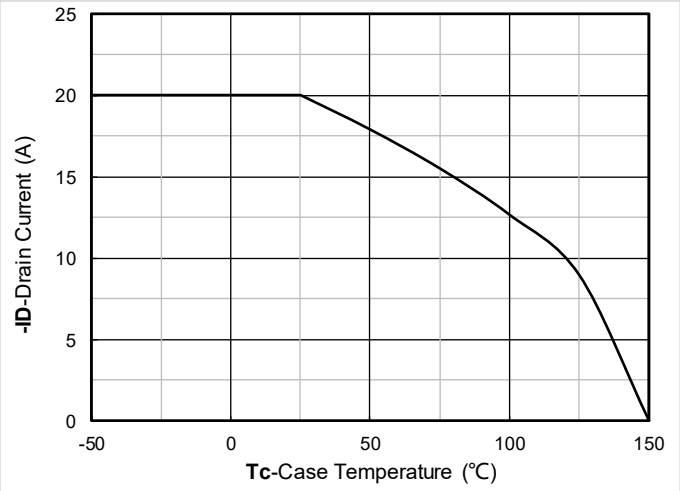



Figure 11. Current dissipation

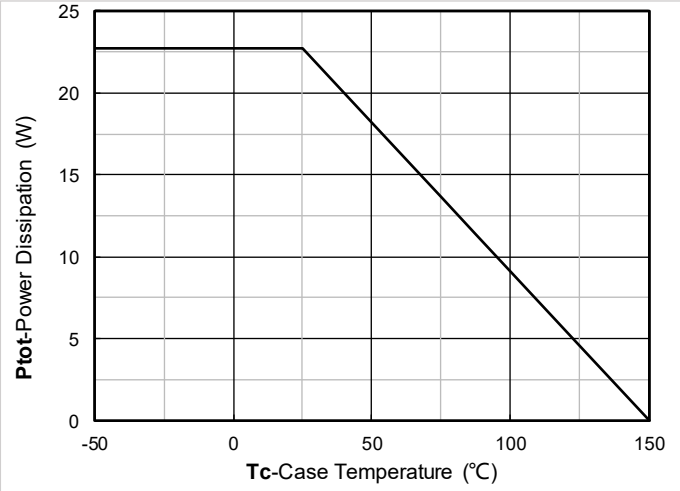



Figure 12. Power dissipation

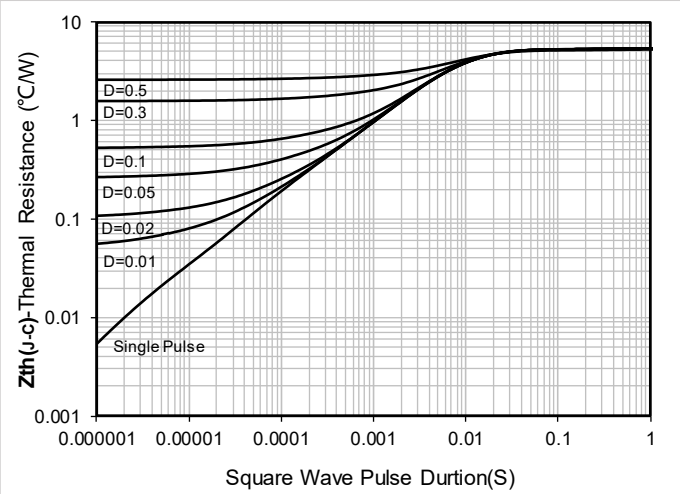



Figure 13. Maximum Transient Thermal Impedance

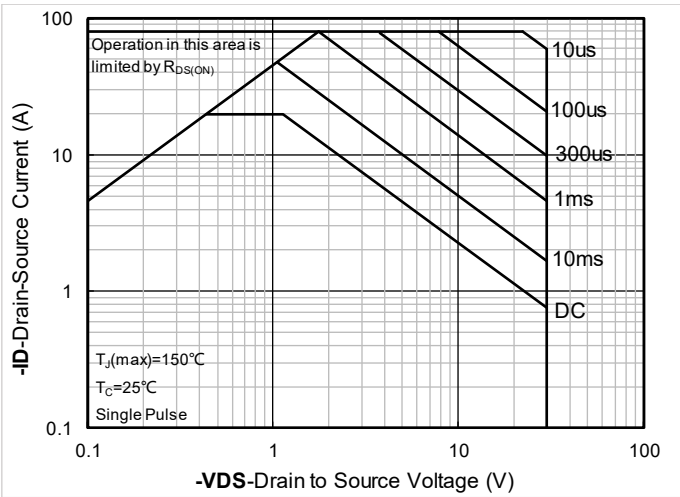
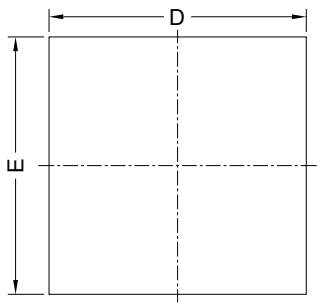
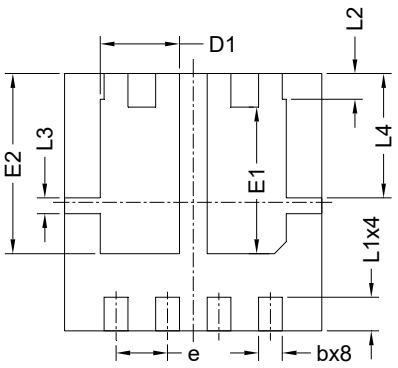



Figure 14. Safe Operation Area

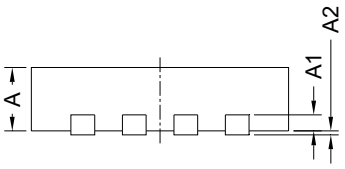
## ■ DFN3333-8L-B-0.8MM Package information



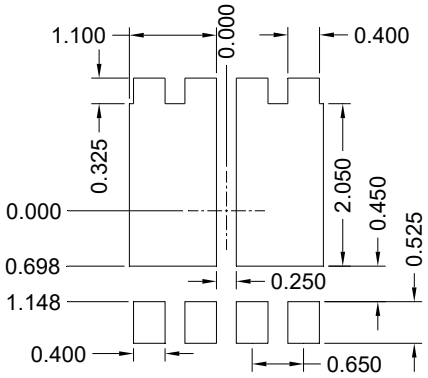

Top View
正面视图




Bottom View
背面视图




Side View
侧面视图




Suggested Solder Pad Layout
Top View

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D | 3.15 | 3.25 | 3.35 |
| E | 3.15 | 3.25 | 3.35 |
| A | 0.70 | 0.80 | 0.90 |
| A1 | | 0.20 BSC | |
| A2 | | | 0.10 |
| D1 | 0.90 | 1.00 | 1.10 |
| E1 | 1.75 | 1.85 | 1.95 |
| E2 | 2.175 | 2.275 | 2.375 |
| L1 | 0.325 | 0.425 | 0.525 |
| L2 | | 0.325 BSC | |
| L3 | | 0.200 BSC | |
| L4 | | 1.570 BSC | |
| b | 0.20 | 0.30 | 0.40 |
| e | | 0.65 BSC | |

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

## Notice

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