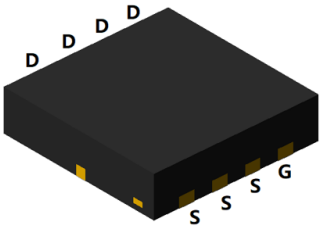
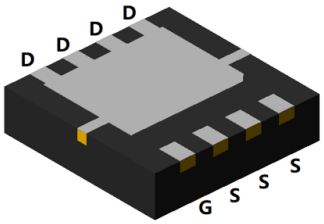
N-Channel Enhancement Mode Field Effect Transistor

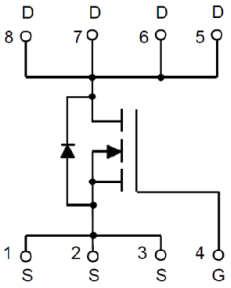


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} 100V
- I_D 40A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜18.5 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜22.5 mohm
- 100% EAS Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC/DC convertor
- Invertors

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	8	A
	T_A=100℃		5	
	T_C=25℃		40	
	T_C =100℃		25.3	
Pulsed Drain Current [A]		I_{DM}	160	A
Avalanche energy [B]		E_{AS}	81	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2	W
	T_A=100℃		0.9	
	T_C=25℃		43	
	T_C =100℃		17.2	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t≤10S	$R_{\theta JA}$	20	25	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		45	55	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.4	2.9	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
Q40G10A	F1	Q40G10A	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		15	18.5	mΩ
		V_{GS}=4.5V, I_D=20A		18	22.5	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.3	V
Maximum Body-Diode Continuous Current	I_S				40	A
Gate resistance	R_G	f=1MHz		1		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHz		1051		pF
Output Capacitance	C_{oss}			399		
Reverse Transfer Capacitance	C_{rss}			18		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=25A		16		nC
Gate-Source Charge	Q_{gs}			5.6		
Gate-Drain Charge	Q_{gd}			2.4		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us		42		
Reverse Recovery Time	t_{rr}			39.8		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,I_{DS}=25A R_{GEN}=2.2Ω		39.2		
Turn-on Rise Time	t_r			11		
Turn-off Delay Time	$t_{D(off)}$			53.2		
Turn-off fall Time	t_f			15.8		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=50V, R_G=25Ω, L=2mH,I_{AS}=9A
C. Pd is based on max. junction temperature, using junction-case thermal resistance.
D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

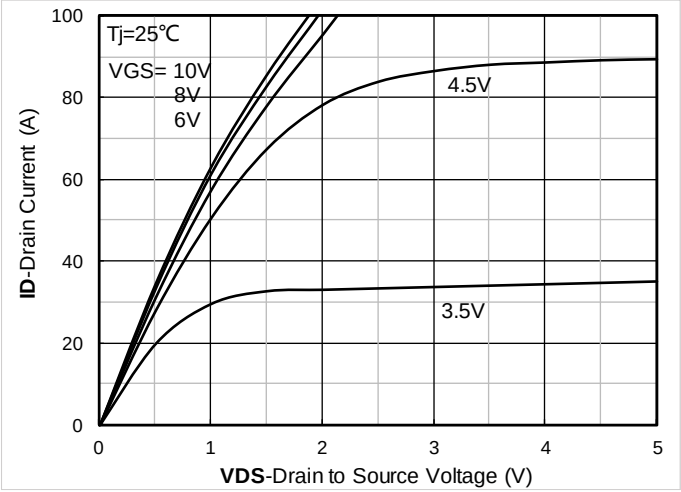


Figure1. Output Characteristics

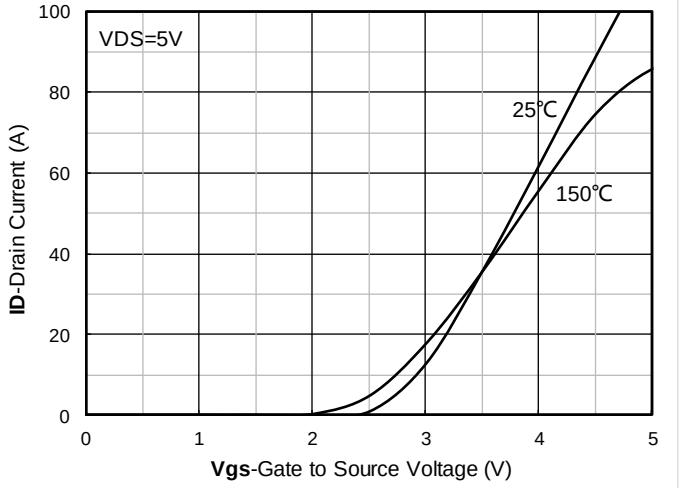


Figure2. Transfer Characteristics

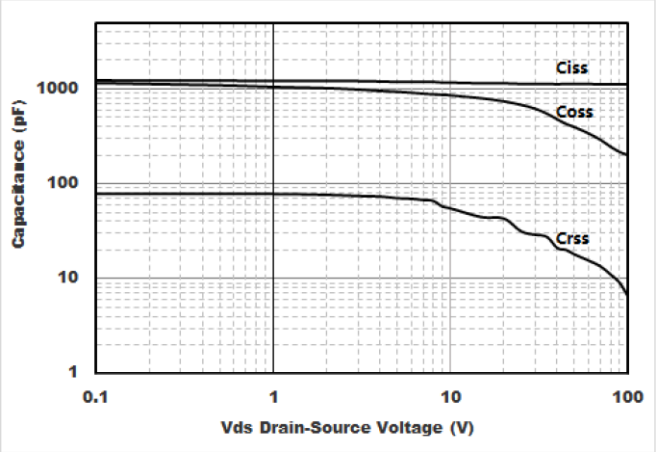


Figure3. Capacitance Characteristics

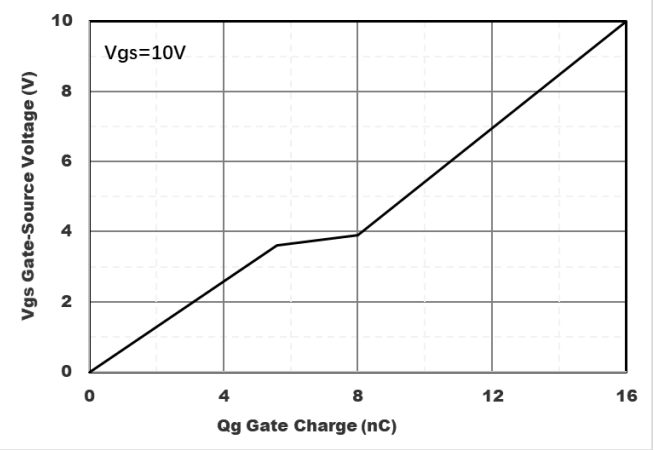


Figure4. Gate Charge

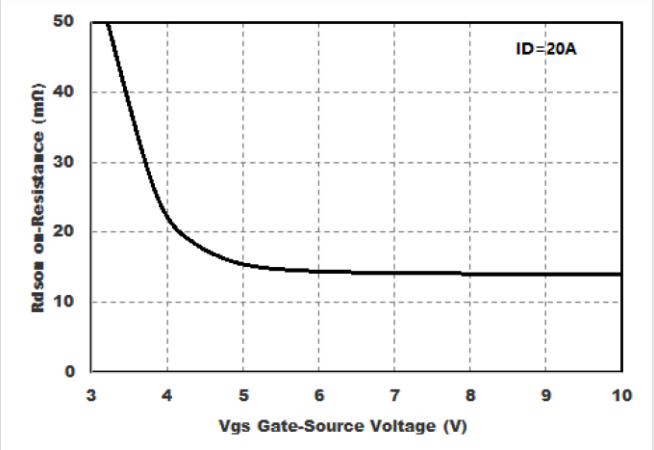


Figure5. **:** On-Resistance vs. Gate to Source Voltage

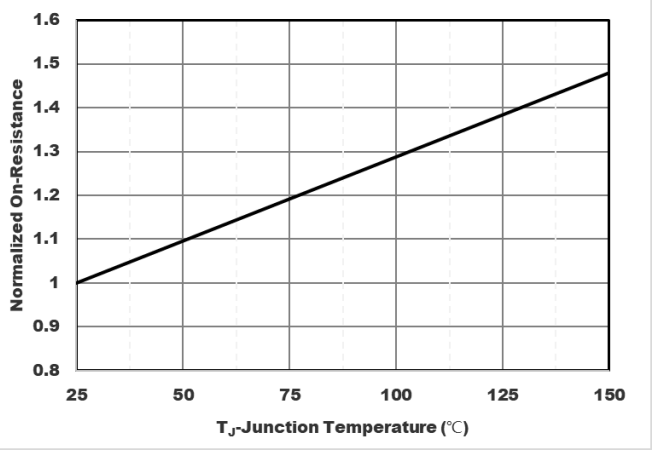


Figure6.Normalized On-Resistance

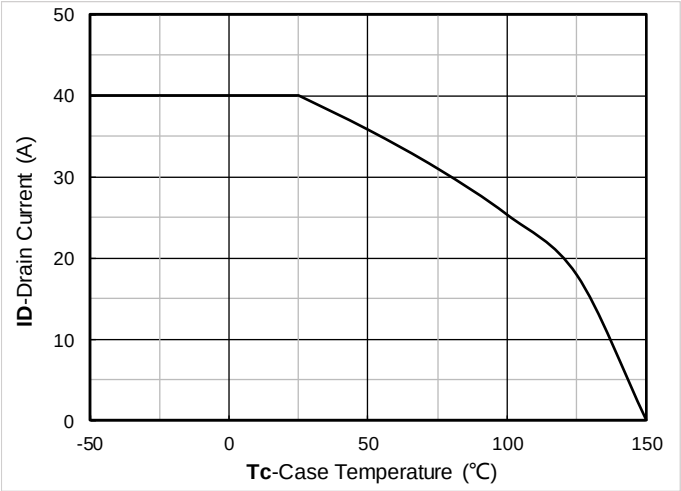


Figure7. Drain current

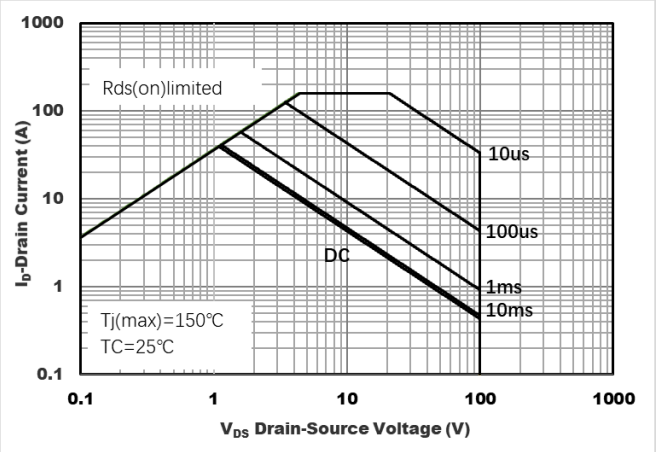


Figure8.Safe Operation Area

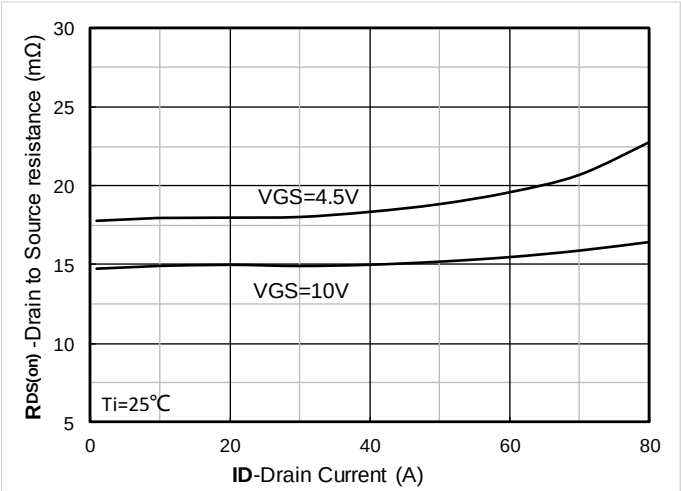


Figure 9. $R_{DS(on)}$ VS Drain Current

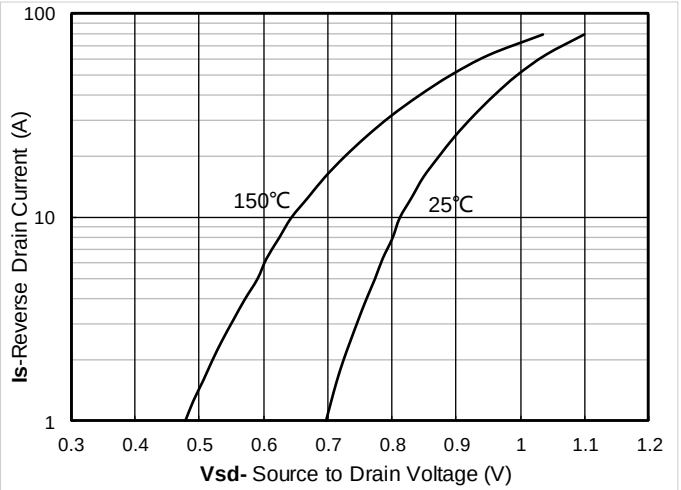


Figure 10. Forward characteristics of reverse diode

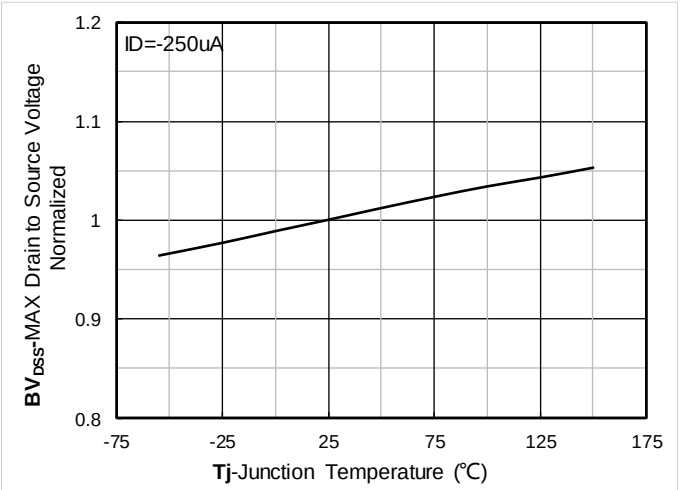


Figure 11. Normalized breakdown voltage

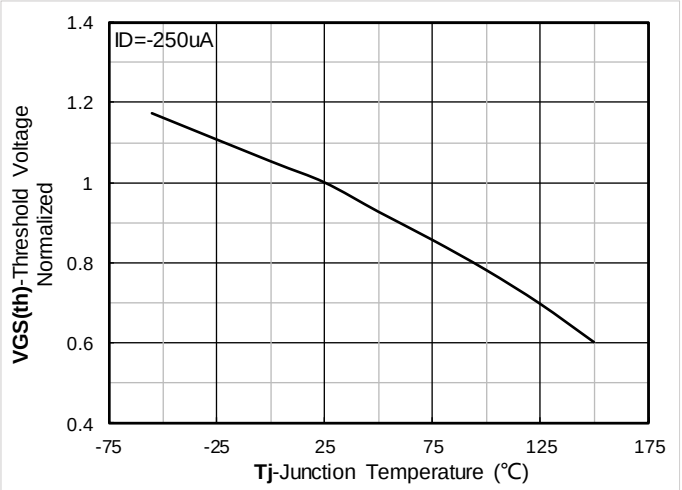


Figure 12. Normalized Threshold voltage

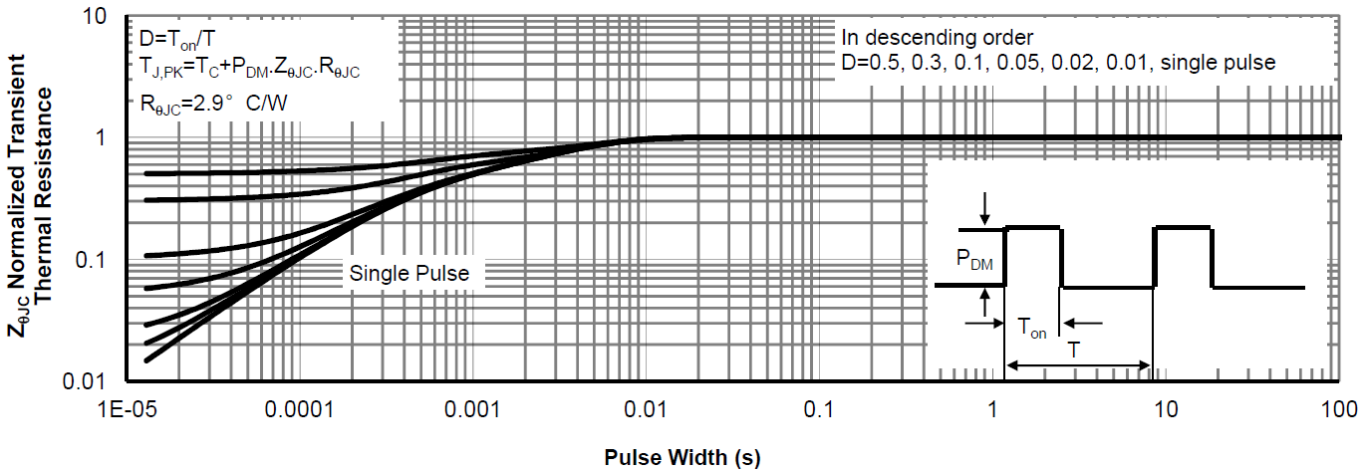
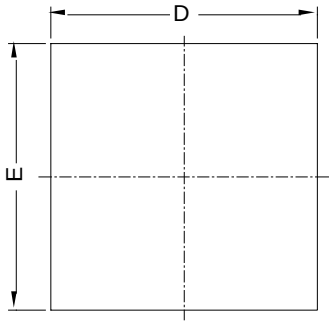
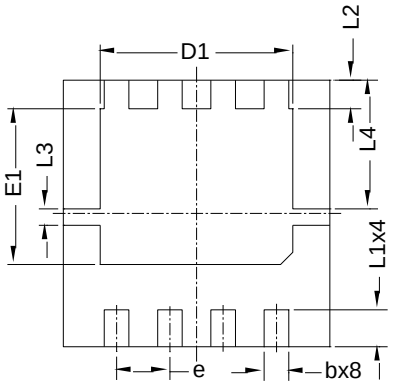


Figure13.Normalized Maximum Transient thermal impedance

■ DFN3333-8L-A Package information



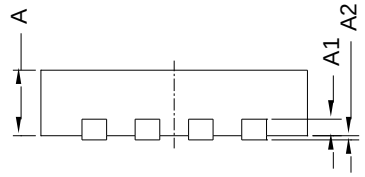
Top View
正面视图



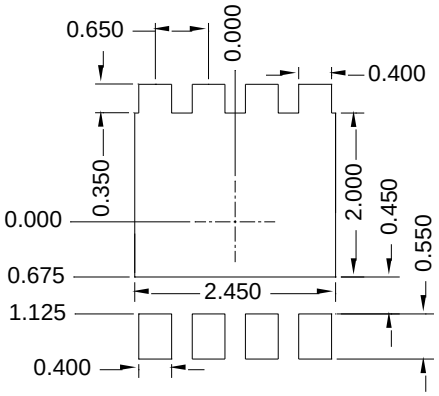
Bottom View
背面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2		0.35 BSC	
L3		0.20 BSC	
L4		1.57 BSC	
b	0.20	0.30	0.40
e		0.65 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.



Side View
侧面视图



Suggested Solder Pad Layout
Top View

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