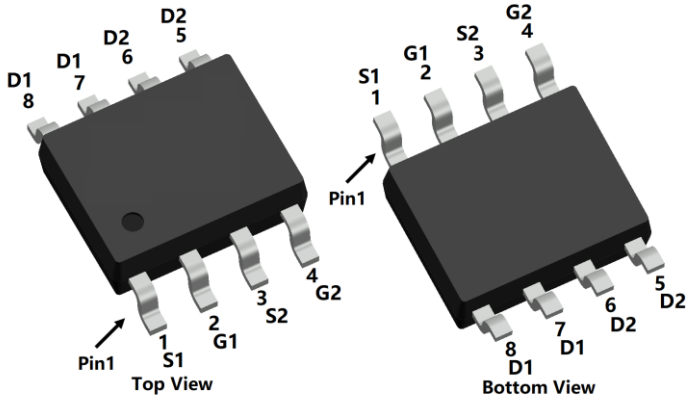
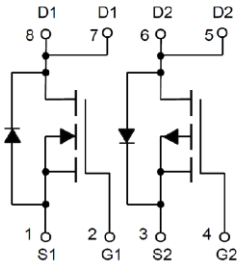
N-Channel and P-Channel Complementary MOSFET



SOP-8



Product Summary

NMOS

- V_{DS} 60V
- I_D 4.4A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜37mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜47mΩ

PMOS

- V_{DS} -60V
- I_D -2.3A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜134mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜180mΩ
- 100% EAS Tested

General Description

- High density cell design for low RDS(ON)
- High Speed switching
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Wireless charger
- Load switch
- Power management

■ Limiting Values

Parameter	Conditions			Symbol	NMOS		PMOS		Unit
					Min	Max	Min	Max	
Drain-source Voltage				V_{DS}	-	60	-	-60	V
Gate-source Voltage				V_{GS}	-20	20	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃	NMOS:V_{GS}=10V, PMOS:V_{GS}=-10V	I_D	-	4.4	-	-2.3	A
		T_A=100℃			-	2.8	-	-1.4	
Pulsed Drain Current	T_A=25℃,t_p≤10μs			I_{DM}	-	35.2	-	-18.4	
Maximum Body-Diode Continuous Current	T_A=25℃			I_S	-	1.2	-	-1.1	
Avalanche Energy (non-repetitive)	NMOS:T_J=25℃,V_G=10V,R_G=25Ω,L=0.5mH,I_{AS}=10A			EAS	-	25	-	12.2	mJ
	PMOS:T_J=25℃,V_G=-10V,R_G=25Ω,L=0.5mH,I_{AS}=-7A								
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃		P_D	-	1.42	-	1.34	W
		T_A=100℃			-	0.56	-	0.53	
Junction and Storage Temperature Range				T_J ,T_{STG}	-55	150	-55	150	℃

■Thermal Resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	88	-	93	℃/W

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
S037NP06A	F2	037NP06A	4000	8000	64000	13“ reel

■ NMOS Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA,Tj=25℃	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=60V,V_{GS}=0V,Tj=150℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	1	1.5	2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=2A,Tj=25℃	-	28	37	mΩ
		V_{GS}=4.5V,I_D=1A,Tj=25℃	-	31.5	47	
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS}=0V,Tj=25℃	-	0.73	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	1.7	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V,f=1MHz,Tj=25℃	-	1173	-	pF
Output Capacitance	C_{oss}		-	65	-	
Reverse Transfer Capacitance	C_{rss}		-	55	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=30V,I_D=2A,Tj=25℃	-	23.4	-	nC
Gate-Source Charge	Q_{gs}		-	2.6	-	
Gate-Drain Charge	Q_{gd}		-	4.3	-	
Reverse Recovery Charge	Q_{rr}	I_F=2A,di/dt=100A/μs,V_{GS}=0V,V_R=30V, Tj=25℃	-	15	-	nC
Reverse Recovery Time	t_{rr}		-	17	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=30V,I_D=2A,R_{GEN}=3Ω, Tj=25℃	-	8.5	-	ns
Turn-on Rise Time	t_r		-	3.3	-	
Turn-off Delay Time	$t_{D(off)}$		-	29	-	
Turn-off Fall Time	t_f		-	3.8	-	

■ PMOS Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA,Tj=25℃	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V,V_{GS}=0V,Tj=25℃	-	-	-1	μA
		V_{DS}=-60V,V_{GS}=0V,Tj=150℃	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA,Tj=25℃	-1	-1.5	-2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-2A,Tj=25℃	-	103	134	mΩ
		V_{GS}=-4.5V,I_D=-1A,Tj=25℃	-	120.6	180	
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS}=0V,Tj=25℃	-	-0.79	-1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	10	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-30V,V_{GS}=0V,f=1MHz,Tj=25℃	-	717	-	pF
Output Capacitance	C_{oss}		-	38.5	-	
Reverse Transfer Capacitance	C_{rss}		-	31.5	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-30V,I_D=-2A,Tj=25℃	-	16.6	-	nC
Gate-Source Charge	Q_{gs}		-	1.6	-	
Gate-Drain Charge	Q_{gd}		-	2.6	-	
Reverse Recovery Charge	Q_{rr}	I_F=-2A,di/dt=100A/us,V_{GS}=0V, V_R=-30V,Tj=25℃	-	22	-	nC
Reverse Recovery Time	t_{rr}		-	19.5	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DS}=-30V,I_D=-2A, R_{GEN}=3Ω,Tj=25℃	-	7	-	ns
Turn-on Rise Time	t_r		-	2.9	-	
Turn-off Delay Time	$t_{D(off)}$		-	27.6	-	
Turn-off Fall Time	t_f		-	5.2	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 80mm*80mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

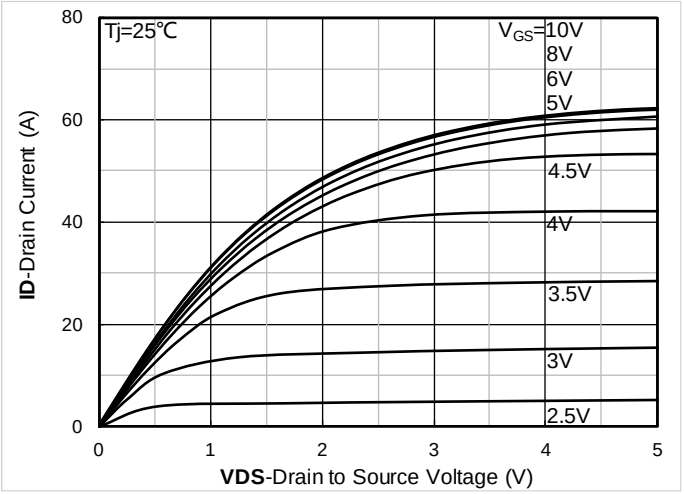


Figure 1. Output Characteristics; typical values

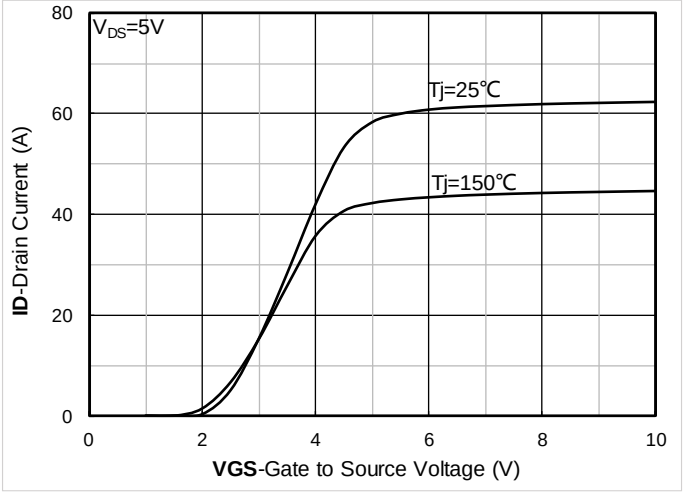


Figure 2. Transfer Characteristics; typical values

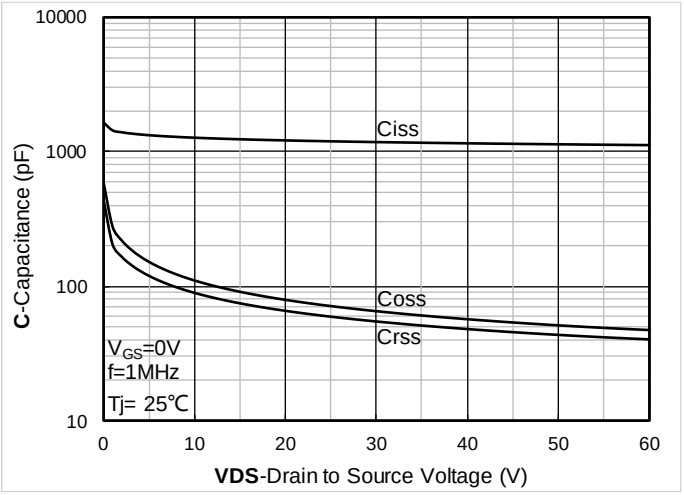


Figure 3. Capacitance Characteristics; typical values

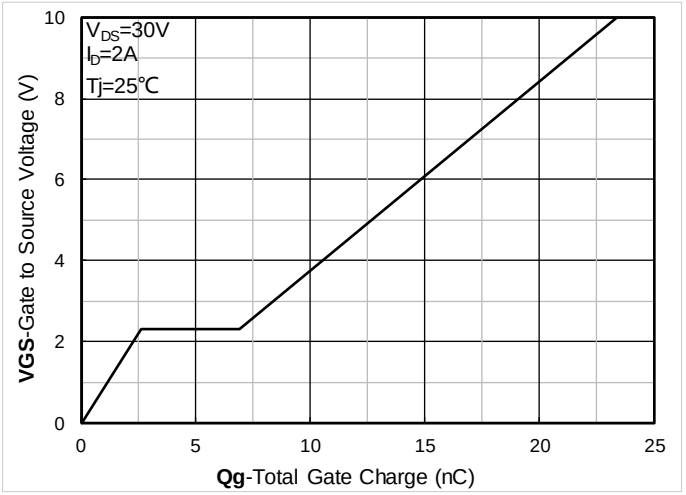


Figure 4. Gate Charge; typical values

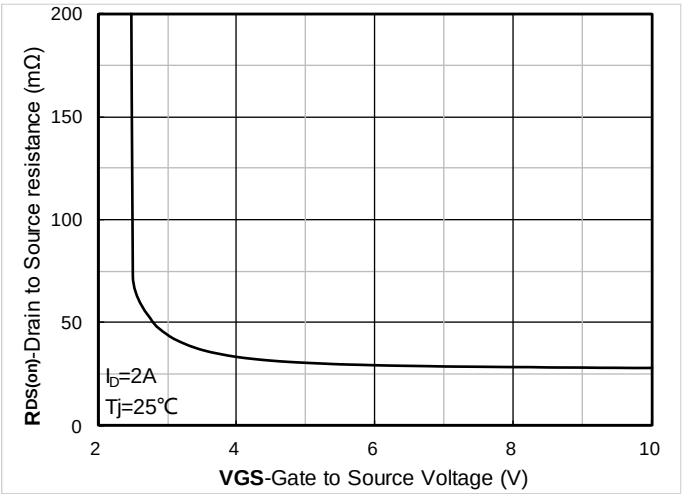


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

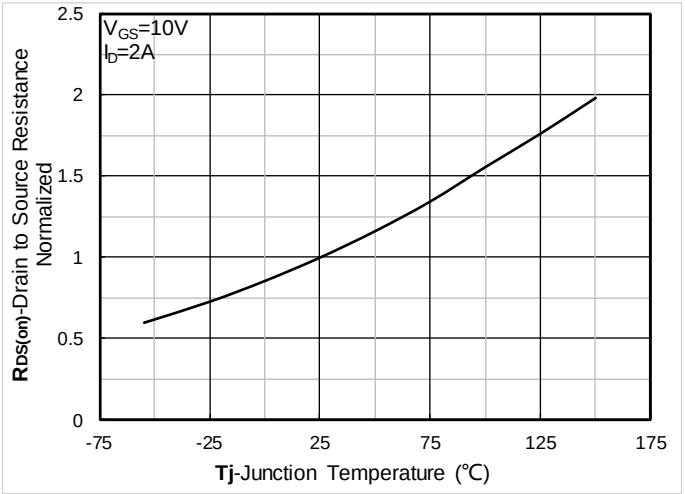


Figure 6. Normalized On-Resistance

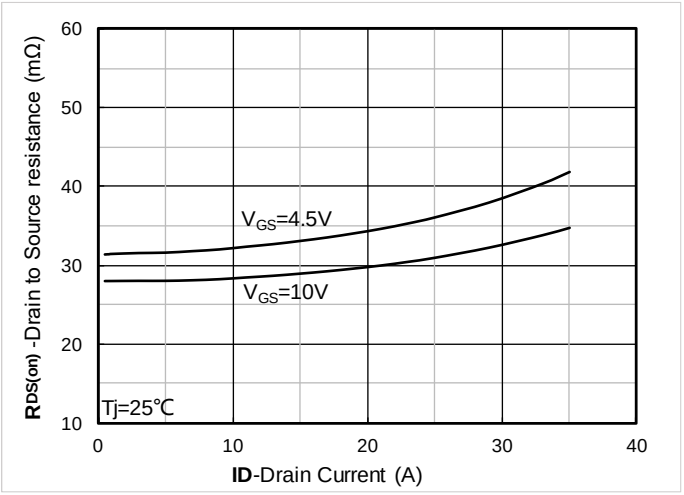


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

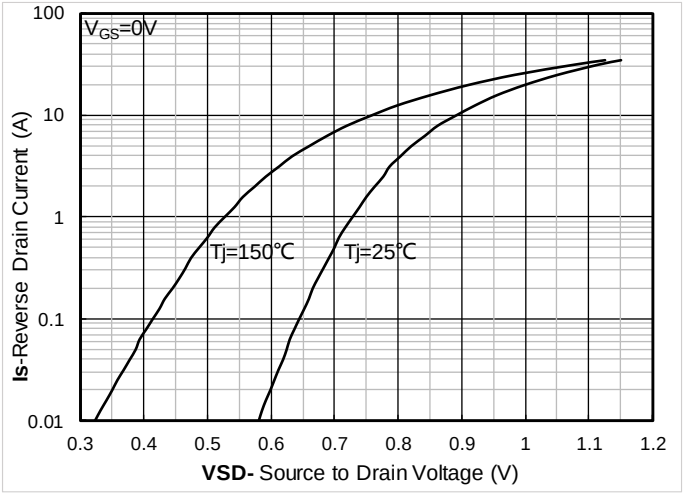


Figure 8. Forward characteristics of reverse diode; typical values

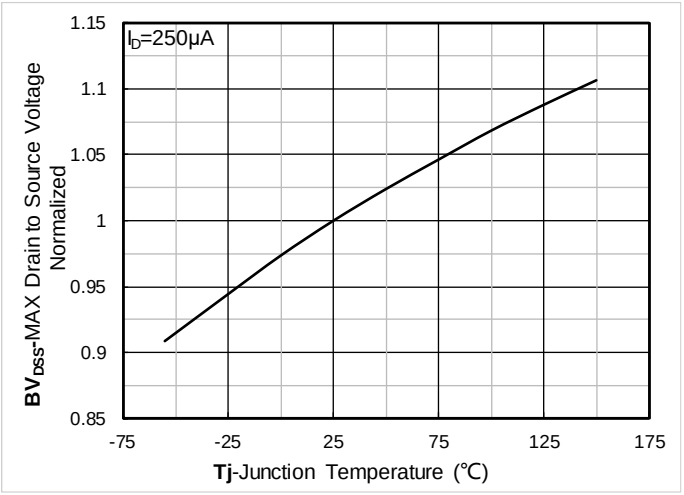


Figure 9. Normalized breakdown voltage

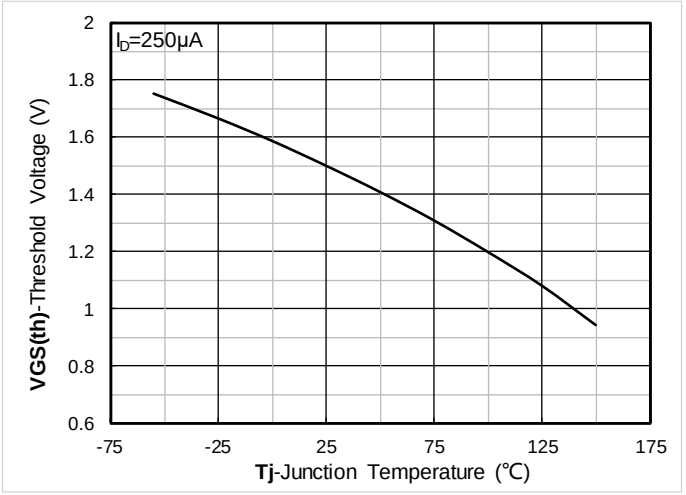


Figure 10. Gate Threshold voltage; typical values

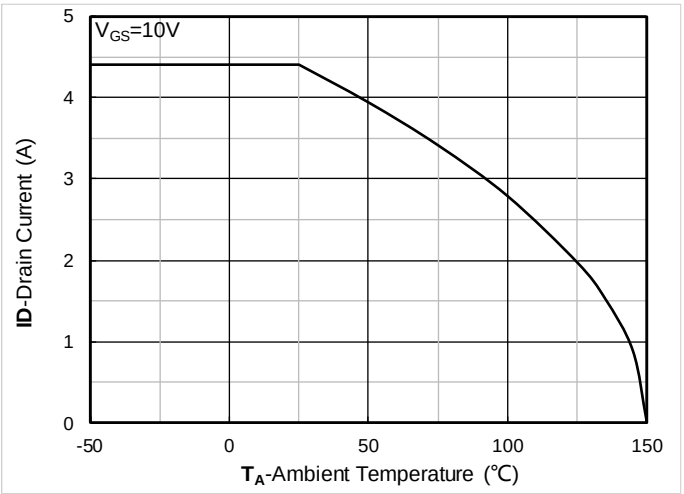


Figure 11. Current dissipation

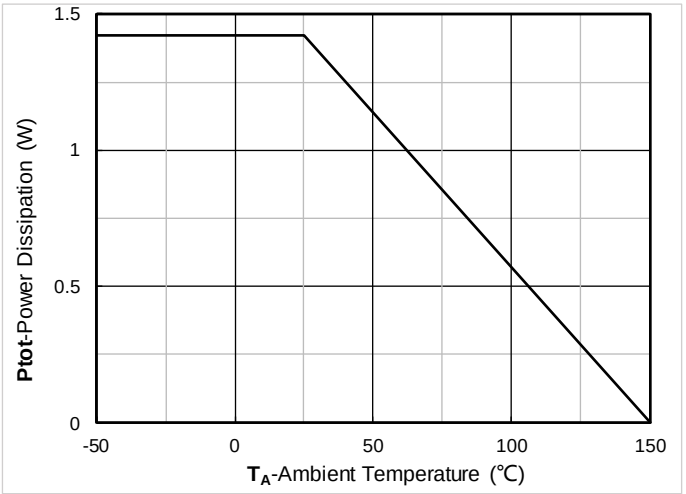


Figure 12. Power dissipation

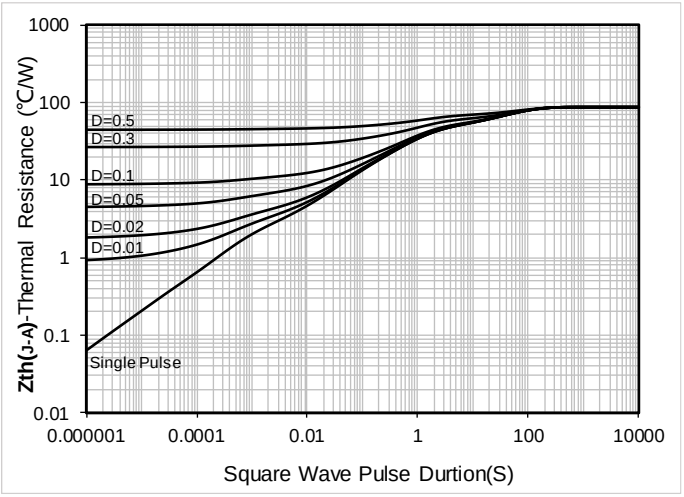


Figure 13. Maximum Transient Thermal Impedance

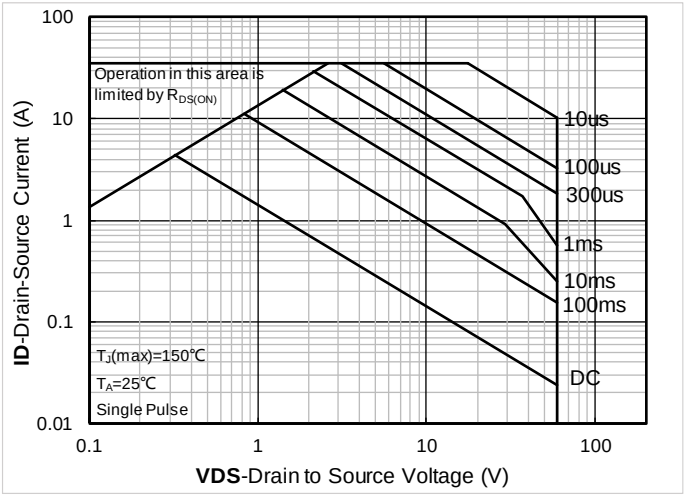


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

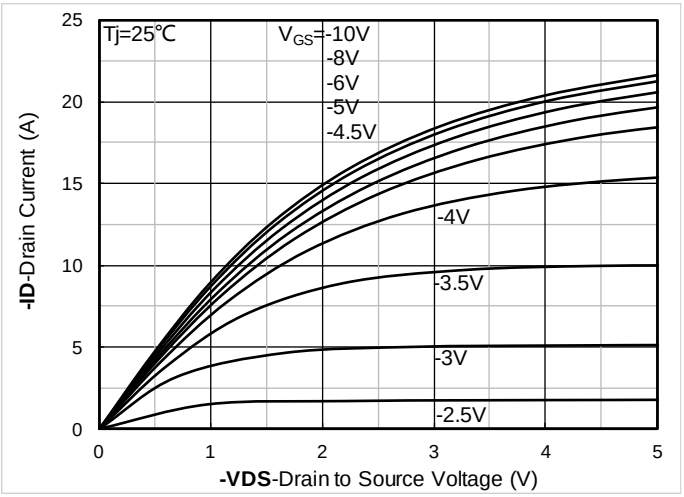


Figure 1. Output Characteristics; typical values

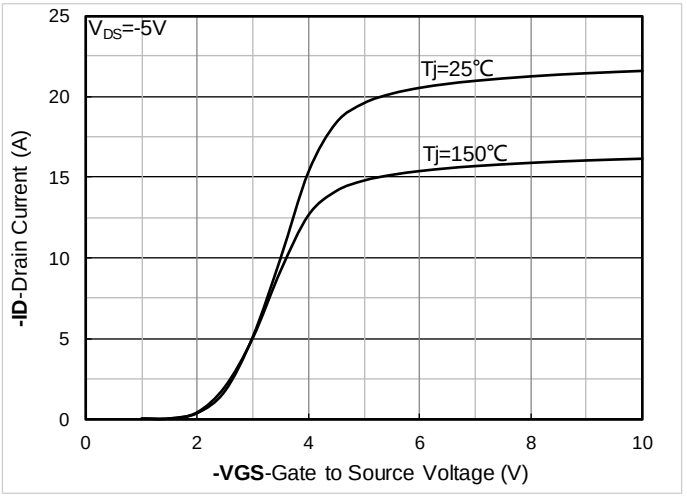


Figure 2. Transfer Characteristics; typical values

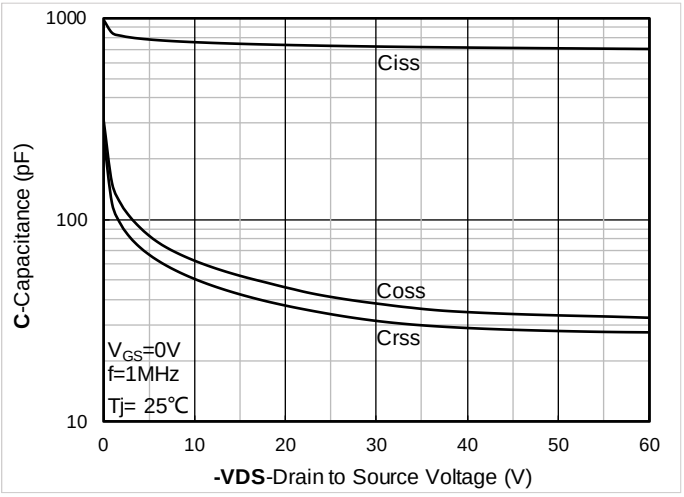


Figure 3. Capacitance Characteristics; typical values

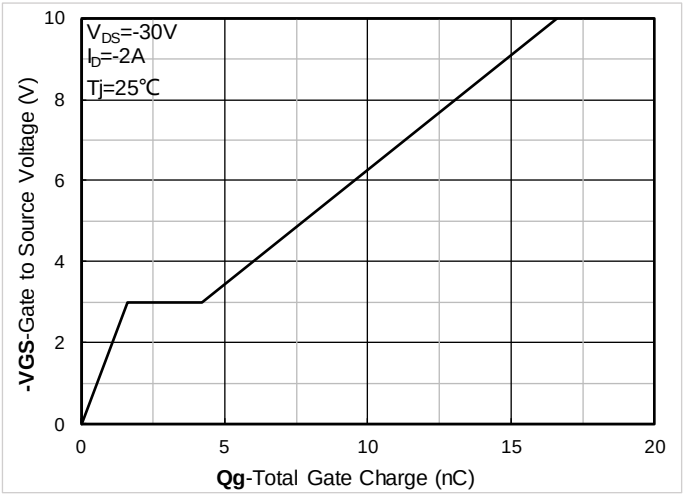


Figure 4. Gate Charge; typical values

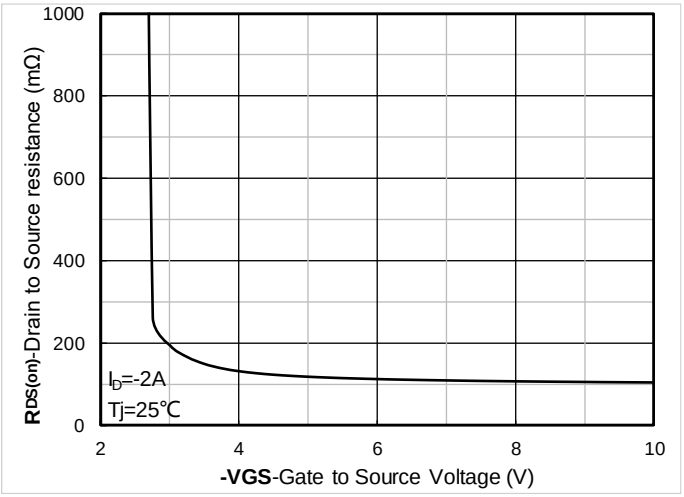


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

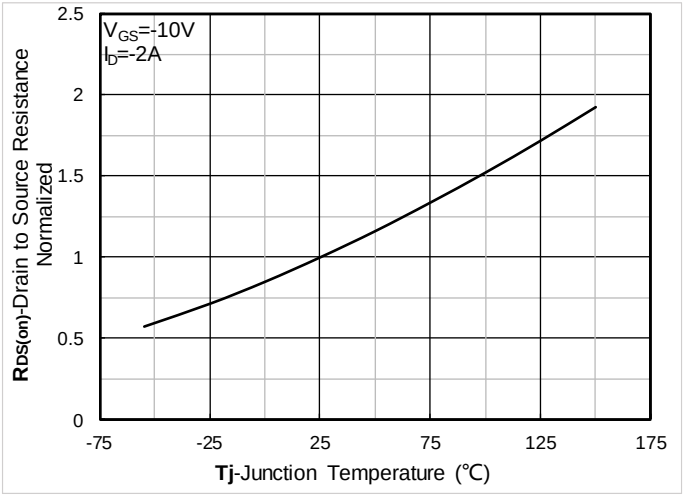


Figure 6. Normalized On-Resistance

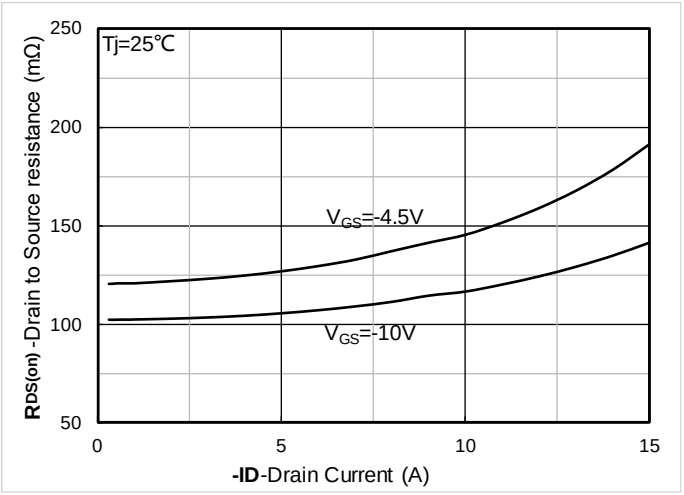


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

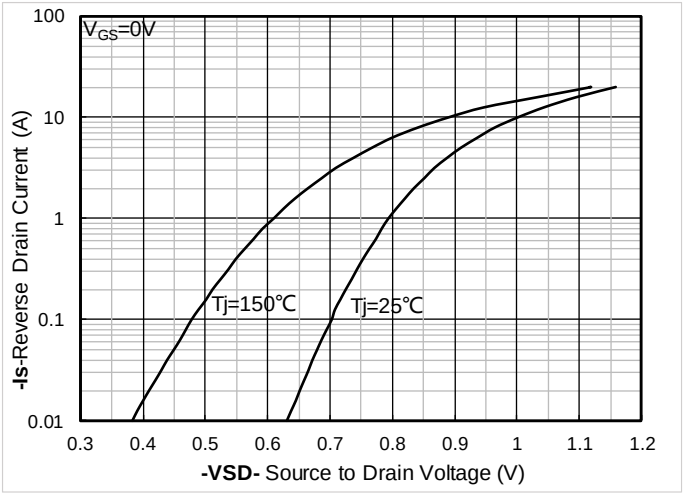


Figure 8. Forward characteristics of reverse diode; typical values

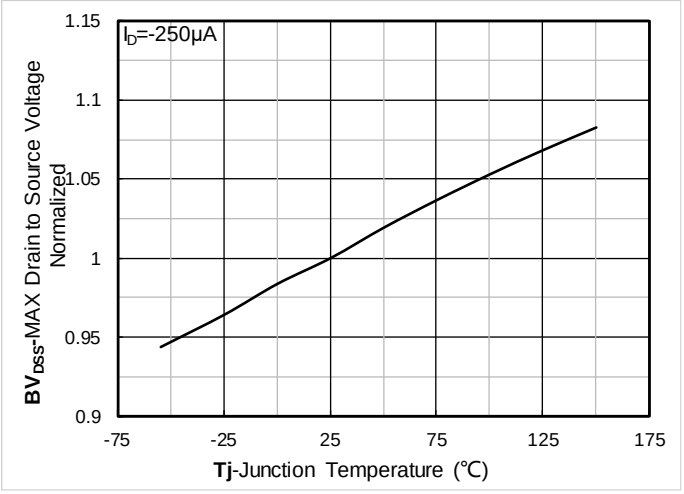


Figure 9. Normalized breakdown voltage

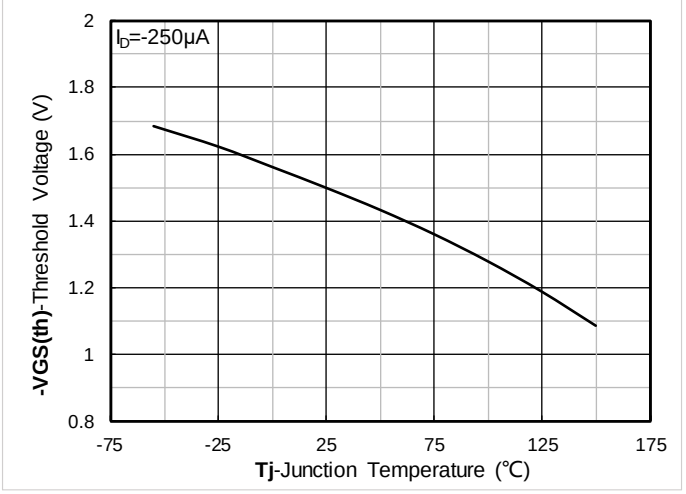


Figure 10. Gate Threshold voltage; typical values

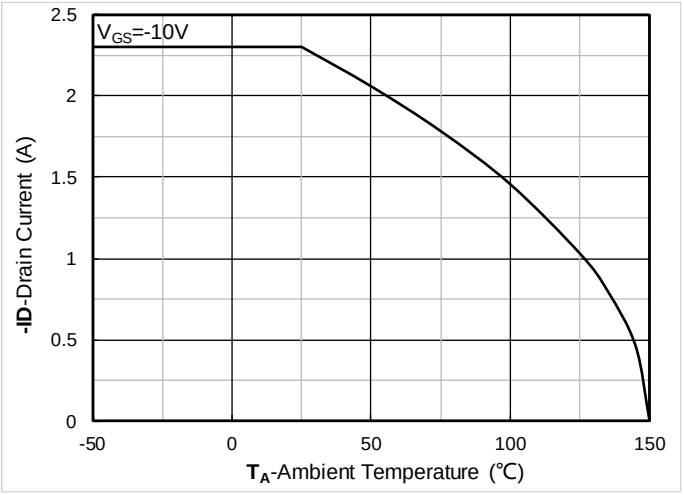


Figure 11. Current dissipation

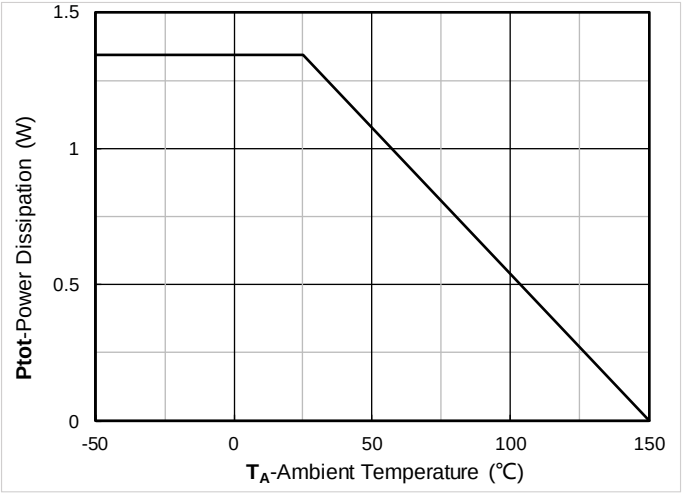


Figure 12. Power dissipation

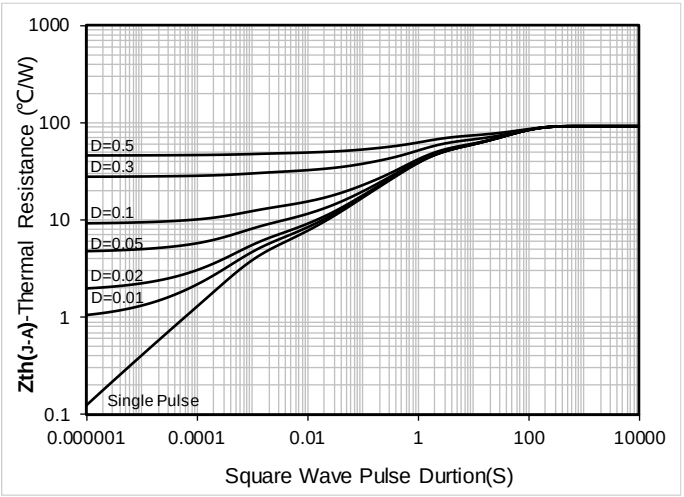


Figure 13. Maximum Transient Thermal Impedance

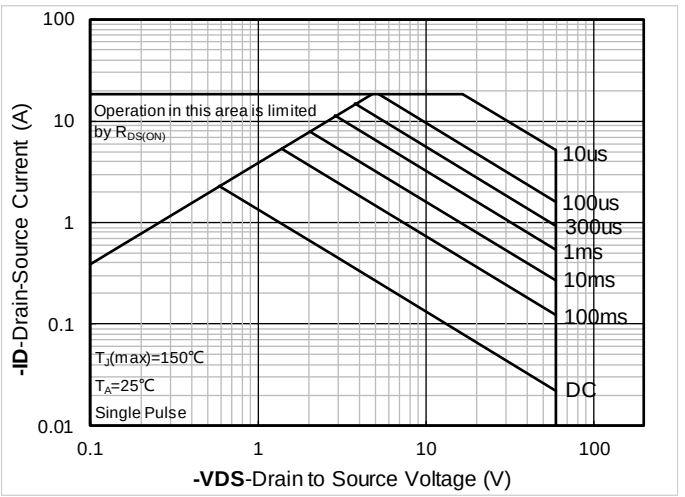
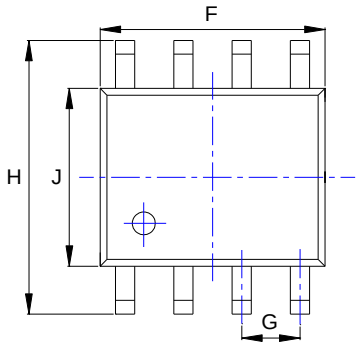
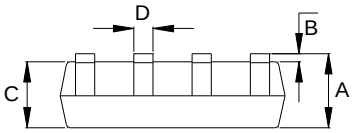


Figure 14. Safe Operation Area

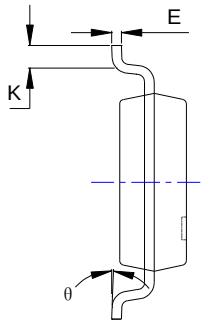
■ SOP-8 Package information



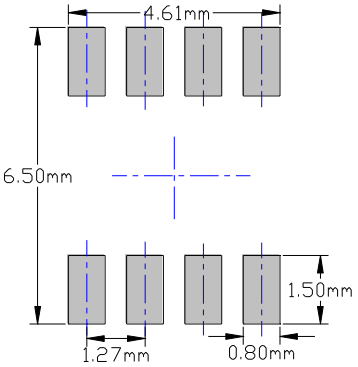
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

Notice

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