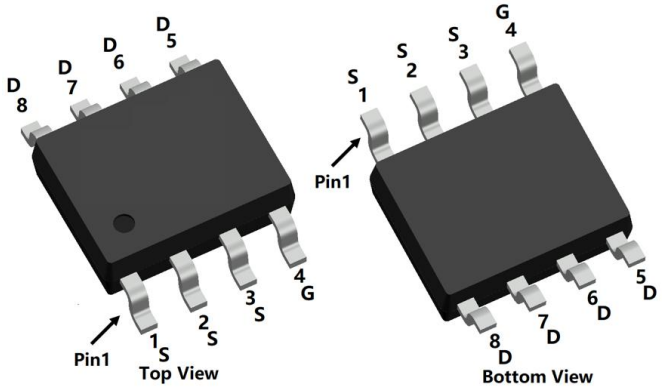
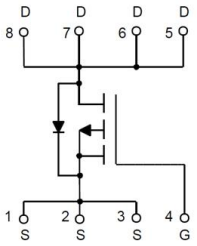
P-Channel Enhancement Mode Field Effect Transistor



SOP-8



Product Summary

- V_{DS} -100V
- I_D -3.3A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜85mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜104mΩ
- 100% EAS Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage	T_J ≥25°C;T_J≤150°C		V_{DS}	-	-100	V
Gate-source Voltage	T_J≤150°C;DC		V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=-10V	I_D	-	-3.3	A
		T_A=100℃,V_{GS}=-10V		-	-2.1	
Pulsed Drain Current	T_A=25℃,t_p≤10μs		I_{DM}	-	-26	
Maximum Body-Diode Continuous Current	T_A=25℃		I_S		-2.4	
Avalanche energy (non-repetitive)	T_J=25℃,V_G=-10V,R_G=25Ω,L=0.5mH,IAS=-16A		EAS	-	64	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	1.9	W
		T_A=100℃		-	0.7	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	150	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	65	℃/W

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
S085P10A	F2	S085P10A	4000	8000	64000	13“ reel

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA,Tj=25℃	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V,Tj=25℃	-	-	-1	μA
		V_{DS}=-100V,V_{GS}=0V,Tj=150℃	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA,Tj=25℃	-1.5	-2.0	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V,I_D=-3A,Tj=25℃	-	72	85	mΩ
		V_{GS}=-4.5V,I_D=-1.5A,Tj=25℃	-	82	104	mΩ
Diode Forward Voltage	V_{SD}	I_S=-3A,V_{GS}=0V,Tj=25℃	-	-0.77	-1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	11	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-50V,V_{GS}=0V,f=1MHz,Tj=25℃	-	2100	-	pF
Output Capacitance	C_{oss}		-	89	-	
Reverse Transfer Capacitance	C_{rss}		-	65	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-50V,I_D=-3A,Tj=25℃	-	46	-	nC
Gate-Source Charge	Q_{gs}		-	5.8	-	
Gate-Drain Charge	Q_{gd}		-	7	-	
Reverse Recovery Charge	Q_{rr}	I_F=-3A,di/dt=100A/μs,V_{GS}=0V, V_R=-50V,Tj=25℃	-	35	-	nC
Reverse Recovery Time	t_{rr}		-	25	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DS}=-50V,I_D=-3A,R_L=16.7Ω, R_{GEN}=3Ω,Tj=25℃	-	8.5	-	ns
Turn-on Rise Time	t_r		-	30.6	-	
Turn-off Delay Time	$t_{D(off)}$		-	116	-	
Turn-off fall Time	t_f		-	42	-	

Note:
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad)

■Typical Electrical and Thermal Characteristics Diagrams

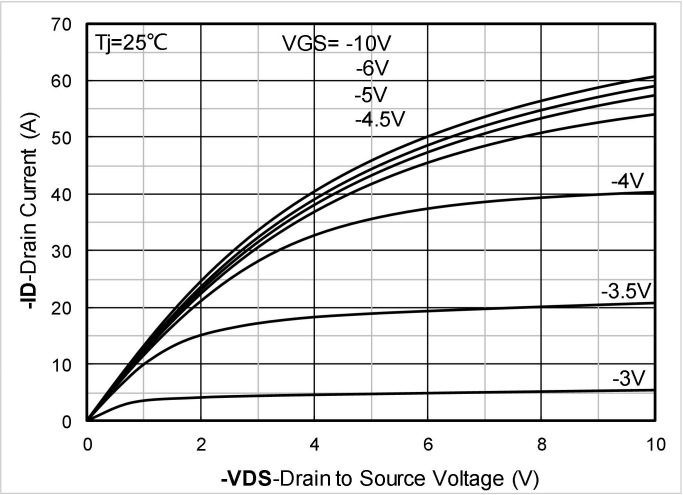


Figure 1. Output Characteristics; typical values

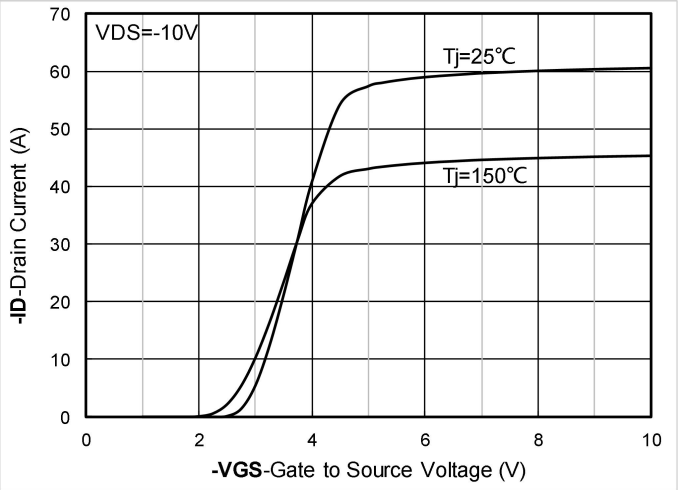


Figure 2. Transfer Characteristics; typical values

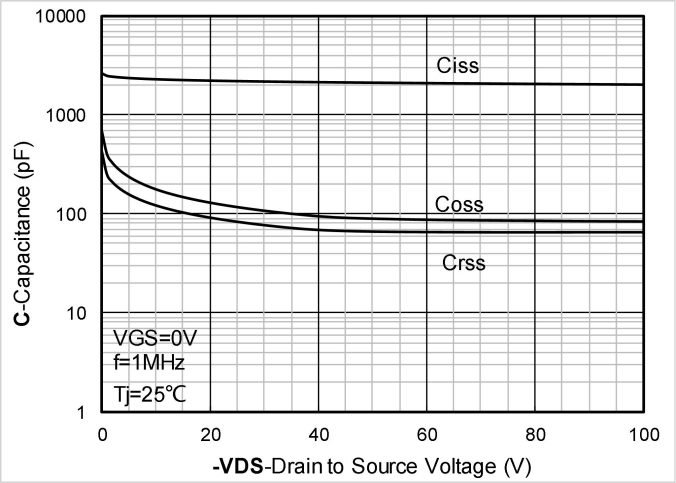


Figure 3. Capacitance Characteristics; typical values

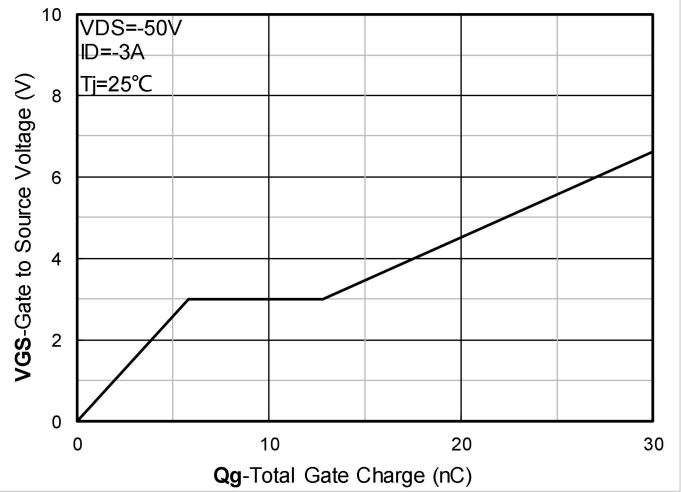


Figure 4. Gate Charge; typical values

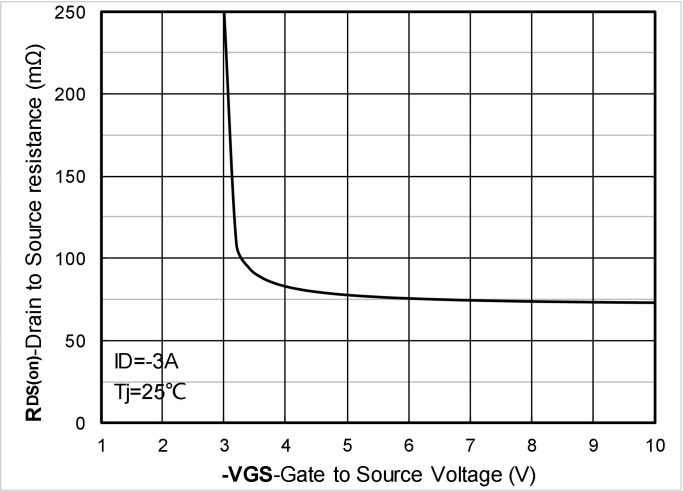


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

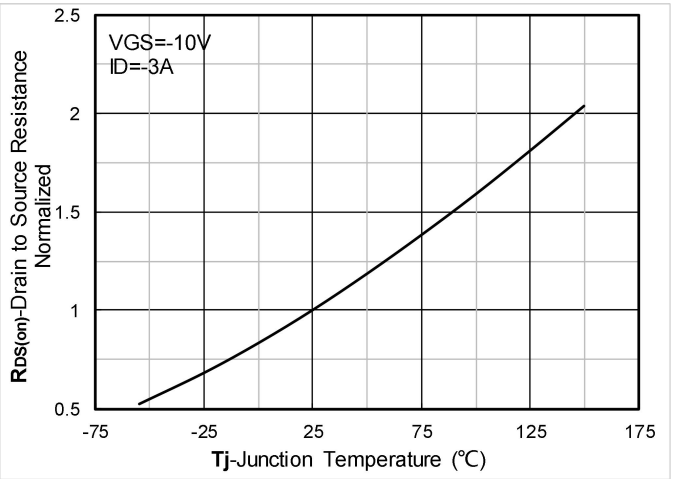


Figure 6. Normalized On-Resistance

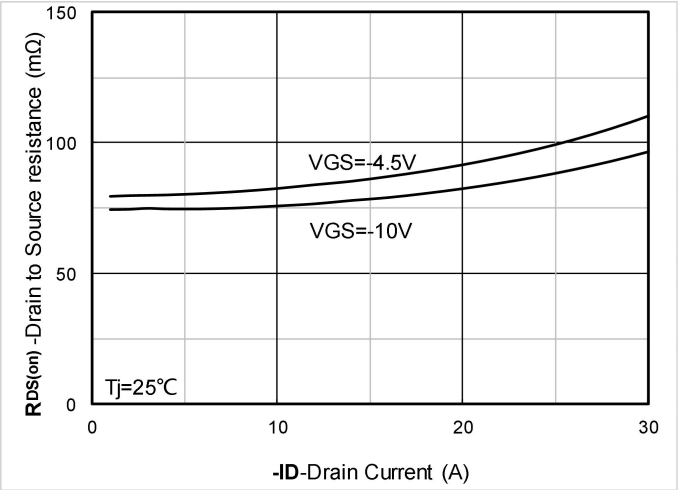


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

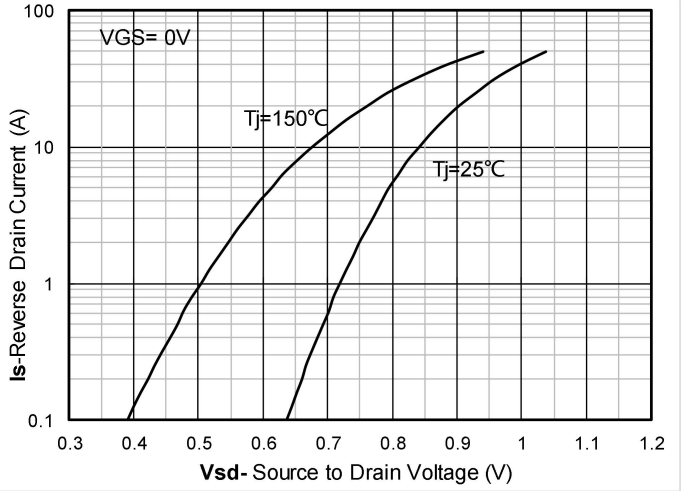


Figure 8. Forward characteristics of reverse diode; typical values

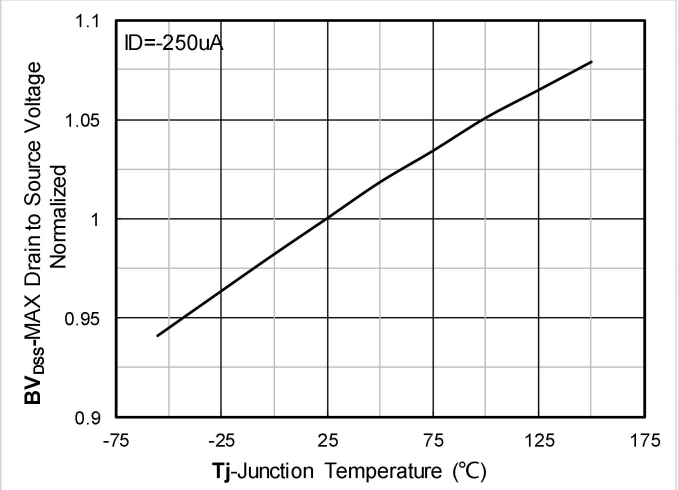


Figure 9. Normalized breakdown voltage

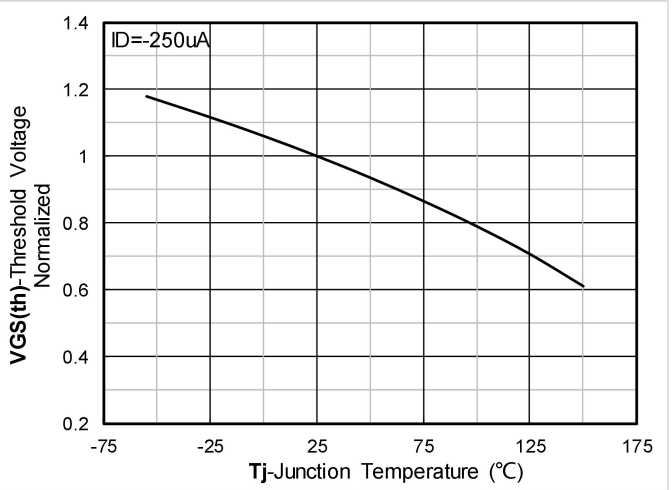


Figure 10. Normalized Threshold voltage

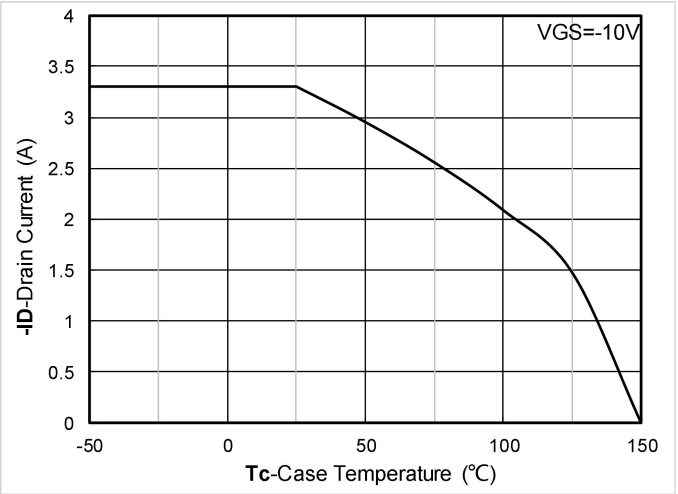


Figure 11. Current dissipation

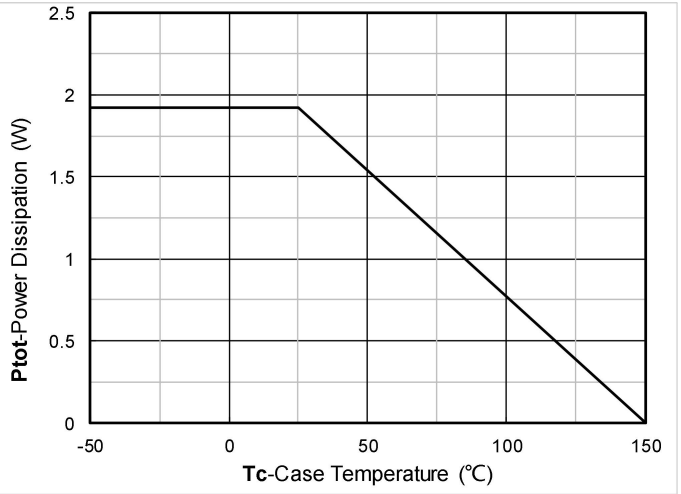


Figure 12. Power dissipation

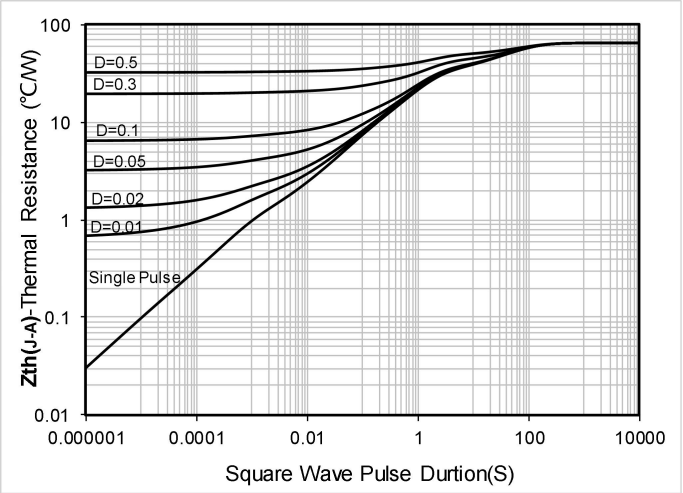


Figure 13. Maximum Transient Thermal Impedance

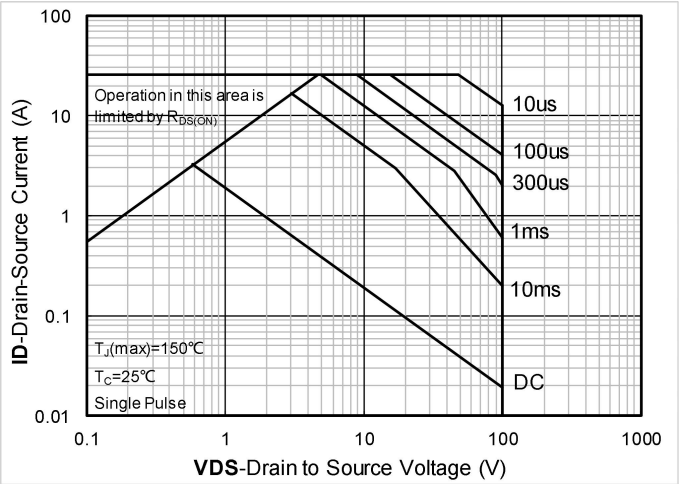
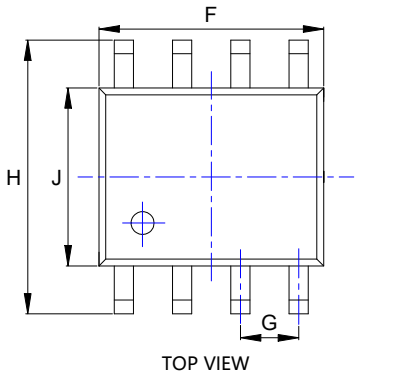
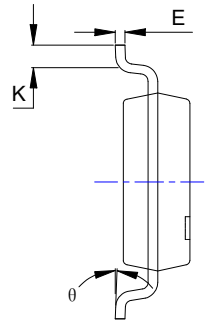


Figure 14. Safe Operation Area

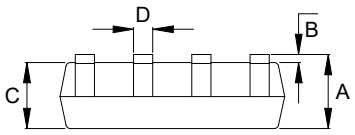
■ SOP-8 Package information



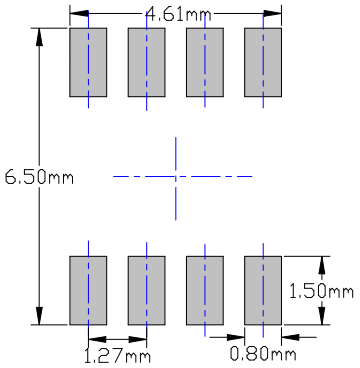
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

Notice

All products, product specifications and data are subject to change without notice to improve reliability, function or design or otherwise.Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in STARSEA's terms and conditions of sale for such products, STARSEA assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of STARSEA products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.