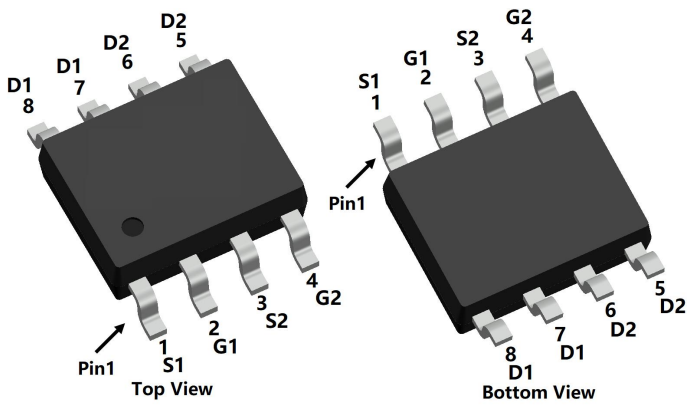
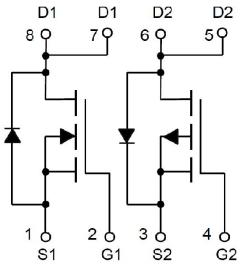
N-Channel and P-Channel Complementary MOSFET



SOP-8



Product Summary

NMOS

- V_{DS} 100V
- I_D 2A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜100mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜110mΩ

PMOS

- V_{DS} -100V
- I_D -1A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜303mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜336mΩ
- 100% EAS Tested

General Description

- High density cell design for low RDS(ON)
- High Speed switching
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Wireless charger
- Load switch
- Power management

■ Limiting Values

Parameter	Conditions			Symbol	NMOS		PMOS		Unit
					Min	Max	Min	Max	
Drain-source Voltage				V_{DS}	-	100	-	-100	V
Gate-source Voltage				V_{GS}	-20	20	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃	NMOS:V_{GS}=10V, PMOS:V_{GS}=-10V	I_D	-	2	-	-1	A
		T_A=100℃			-	1.26	-	-0.63	
Pulsed Drain Current	T_A=25℃,t_p≤10μs			I_{DM}	-	16	-	-8	
Maximum Body-Diode Continuous Current	T_A=25℃			I_S	-	1.4	-	-1	
Avalanche Energy (non-repetitive)	NMOS:T_J=25℃,V_G=10V,R_G=25Ω,L=0.5mH,I_{AS}=6.58A			EAS	-	10.8	-	12.2	mJ
	PMOS:T_J=25℃,V_G=-10V,R_G=25Ω,L=0.5mH,I_{AS}=-7A								
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃		P_D	-	1.25	-	1.25	W
		T_A=100℃			-	0.5	-	0.5	
Junction and Storage Temperature Range				T_J ,T_{STG}	-55	150	-55	150	℃

■Thermal Resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	100	-	100	℃/W

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
S100NP10AJ	F2	100NP10	4000	8000	64000	13“ reel

■ NMOS Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA,Tj=25℃	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=100V,V_{GS}=0V,Tj=150℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	1.3	1.8	2.3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=2A,Tj=25℃	-	77	100	mΩ
		V_{GS}=4.5V,I_D=1A,Tj=25℃	-	84	110	
Diode Forward Voltage	V_{SD}	I_S=1.4A,V_{GS}=0V,Tj=25℃	-	0.75	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	1.7	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHz,Tj=25℃	-	903	-	pF
Output Capacitance	C_{oss}		-	30	-	
Reverse Transfer Capacitance	C_{rss}		-	28	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=2A,Tj=25℃	-	23.2	-	nC
Gate-Source Charge	Q_{gs}		-	2.6	-	
Gate-Drain Charge	Q_{gd}		-	6.1	-	
Reverse Recovery Charge	Q_{rr}	I_F=2A,di/dt=100A/μs,V_{GS}=0V,V_R=50V, Tj=25℃	-	25	-	nC
Reverse Recovery Time	t_{rr}		-	22	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=50V,I_D=2A,R_{GEN}=3Ω, Tj=25℃	-	7.4	-	ns
Turn-on Rise Time	t_r		-	3.4	-	
Turn-off Delay Time	$t_{D(off)}$		-	28.6	-	
Turn-off Fall Time	t_f		-	4.3	-	

■ PMOS Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA,Tj=25℃	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V,Tj=25℃	-	-	-1	μA
		V_{DS}=-100V,V_{GS}=0V,Tj=150℃	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA,Tj=25℃	-1	-1.5	-2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-1A,Tj=25℃	-	233	303	mΩ
		V_{GS}=-4.5V,I_D=-1A,Tj=25℃	-	249	336	
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS}=0V,Tj=25℃	-	-0.79	-1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	5	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-50V,V_{GS}=0V,f=1MHz,Tj=25℃	-	965	-	pF
Output Capacitance	C_{oss}		-	23	-	
Reverse Transfer Capacitance	C_{rss}		-	21	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-50V,I_D=-1A,Tj=25℃	-	19	-	nC
Gate-Source Charge	Q_{gs}		-	4.6	-	
Gate-Drain Charge	Q_{gd}		-	1.8	-	
Reverse Recovery Charge	Q_{rr}	I_F=-1A,di/dt=100A/us,V_{GS}=0V, V_R=-50V,Tj=25℃	-	18	-	nC
Reverse Recovery Time	t_{rr}		-	21	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DS}=-50V,I_D=-1A, R_{GEN}=3.9Ω,Tj=25℃	-	5.8	-	ns
Turn-on Rise Time	t_r		-	2.8	-	
Turn-off Delay Time	$t_{D(off)}$		-	28	-	
Turn-off Fall Time	t_f		-	18	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

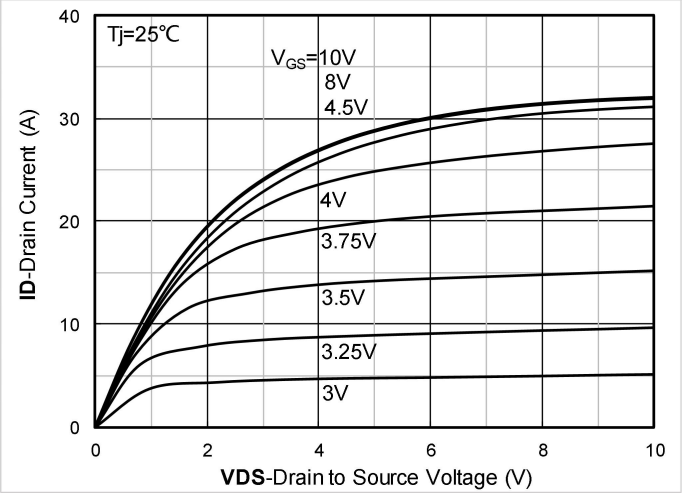


Figure 1. Output Characteristics; typical values

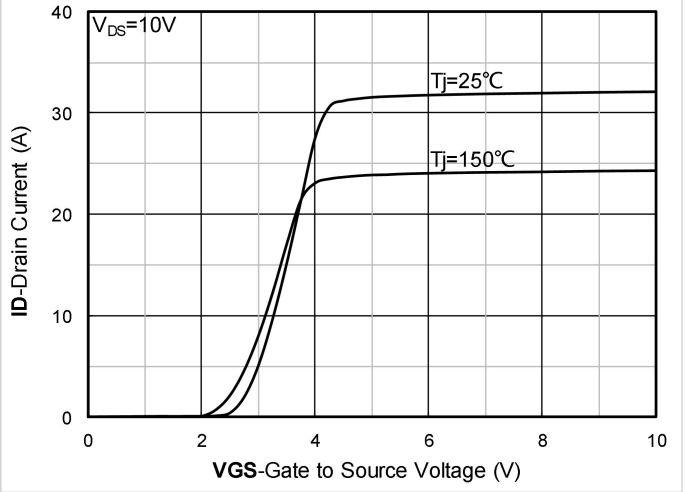


Figure 2. Transfer Characteristics; typical values

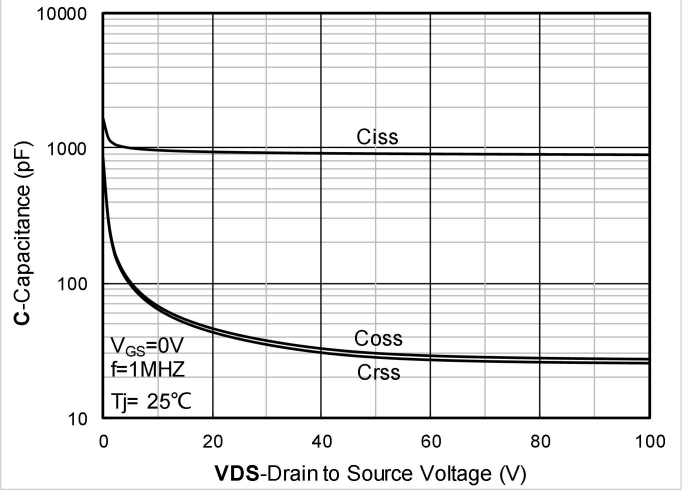


Figure 3. Capacitance Characteristics; typical values

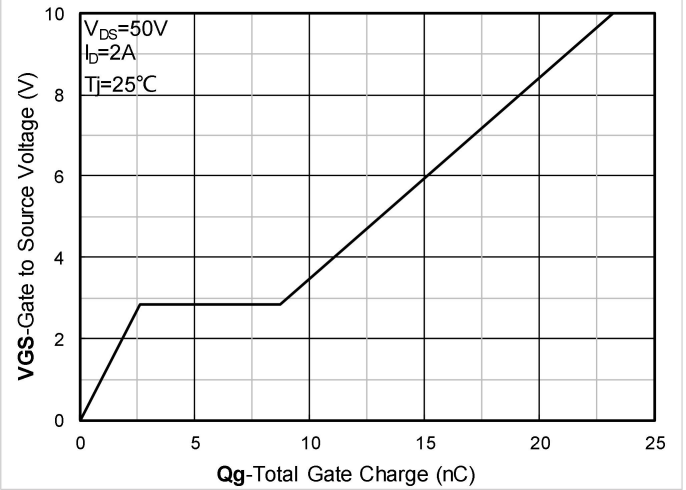


Figure 4. Gate Charge; typical values

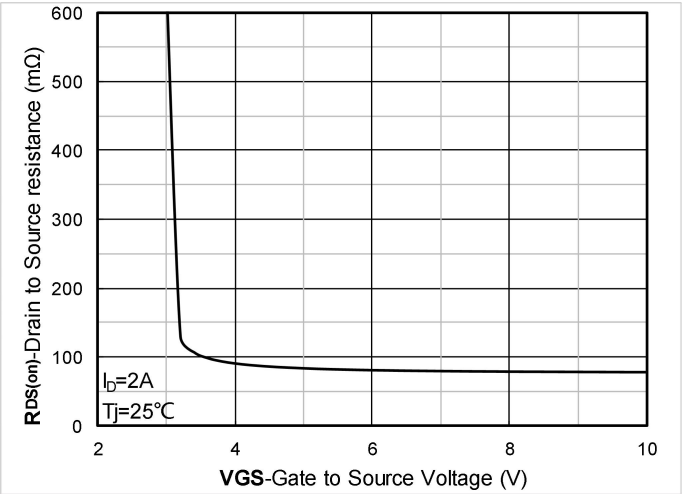


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

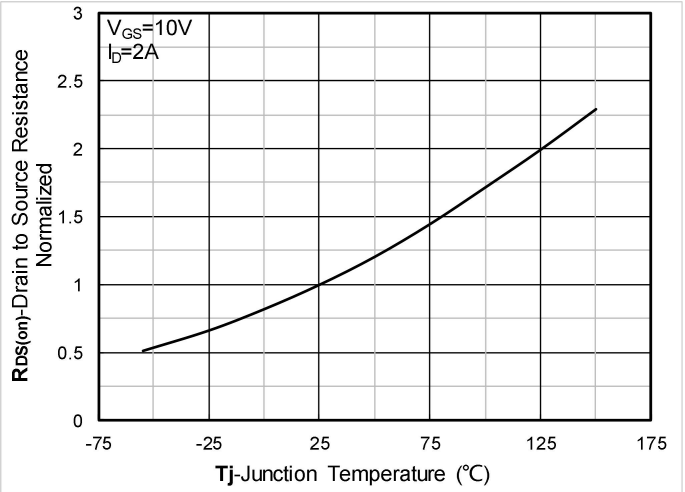


Figure 6. Normalized On-Resistance

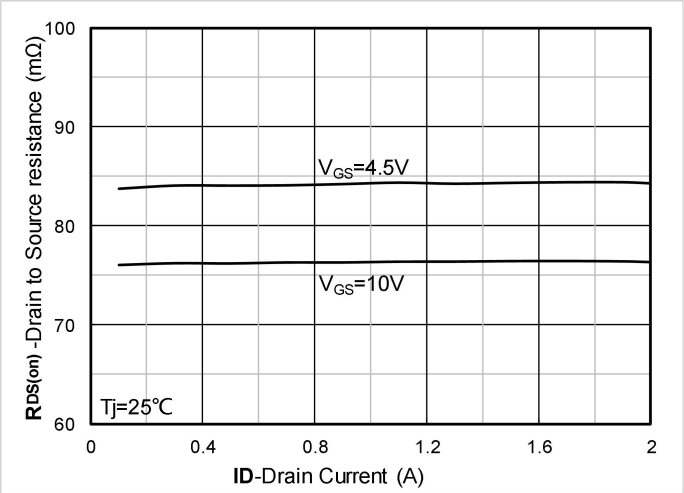


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

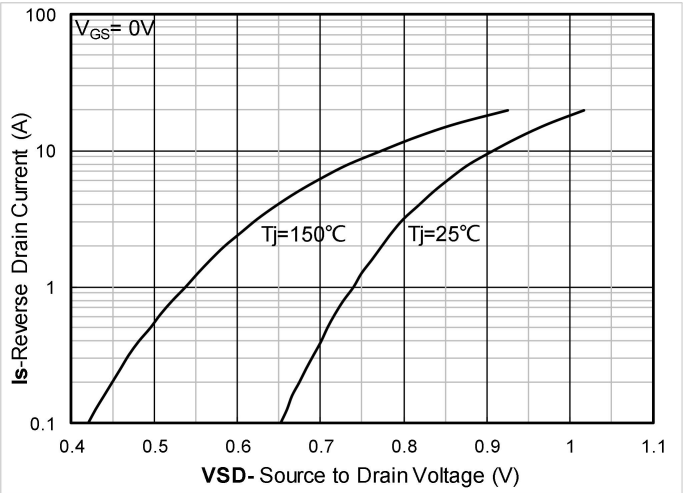


Figure 8. Forward characteristics of reverse diode; typical values

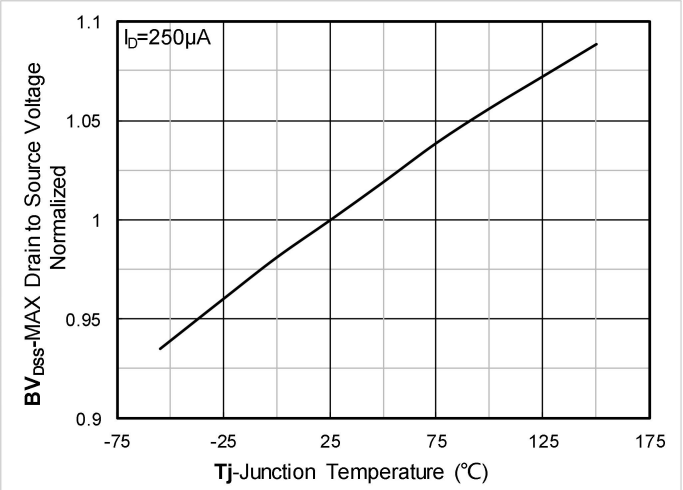


Figure 9. Normalized breakdown voltage

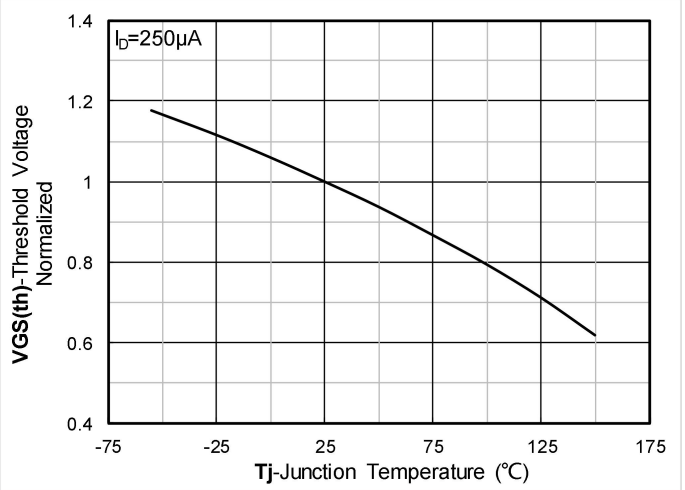


Figure 10. Normalized Threshold voltage

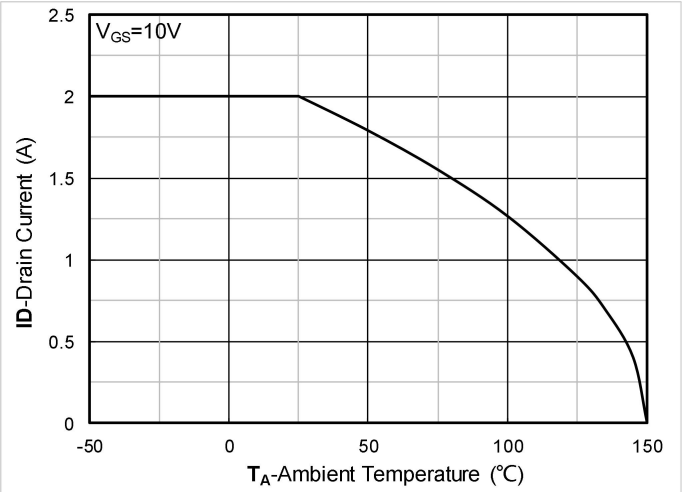


Figure 11. Current dissipation

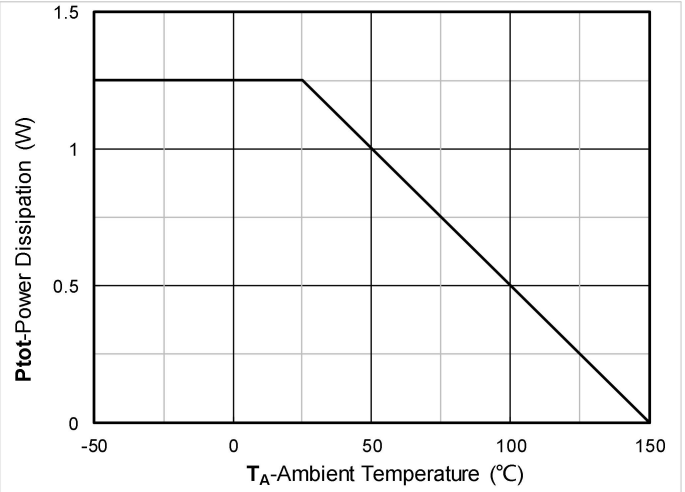


Figure 12. Power dissipation

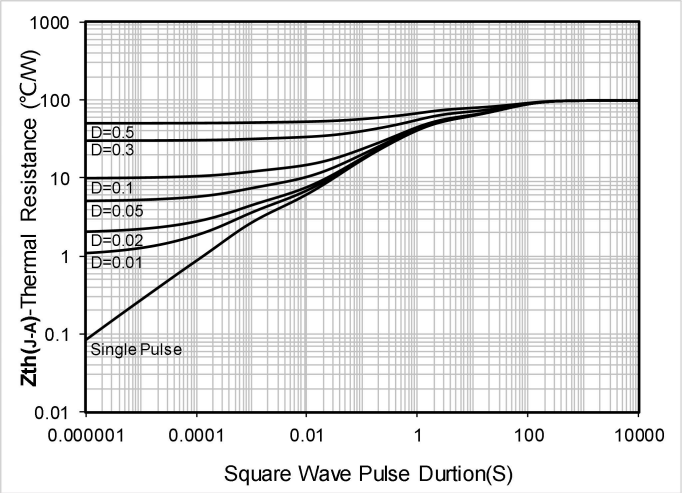


Figure 13. Maximum Transient Thermal Impedance

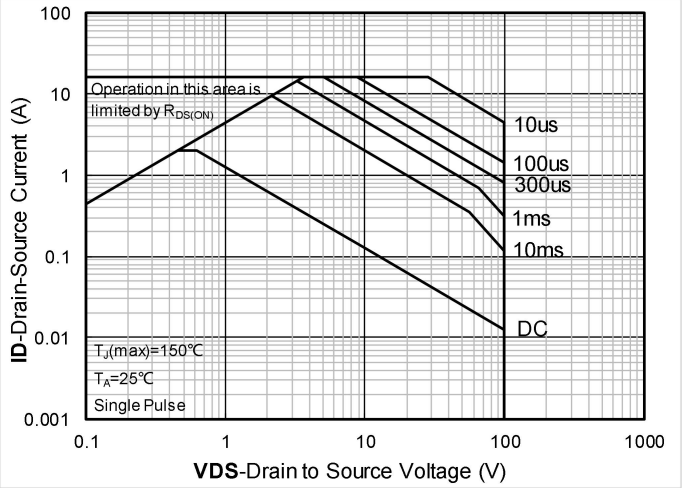


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

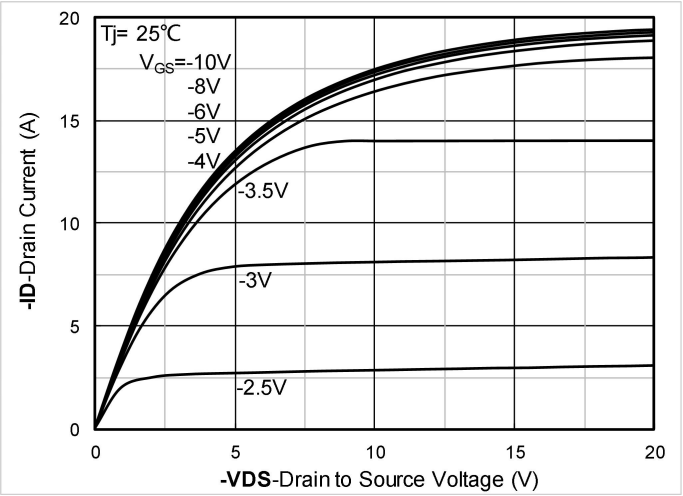


Figure 1. Output Characteristics; typical values

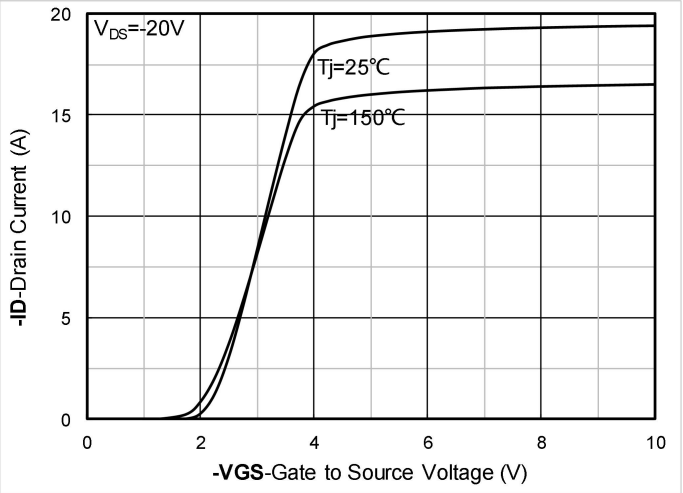


Figure 2. Transfer Characteristics; typical values

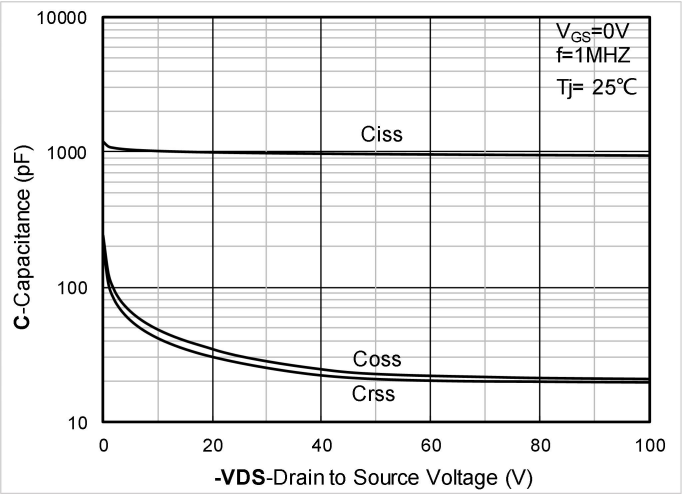


Figure 3. Capacitance Characteristics; typical values

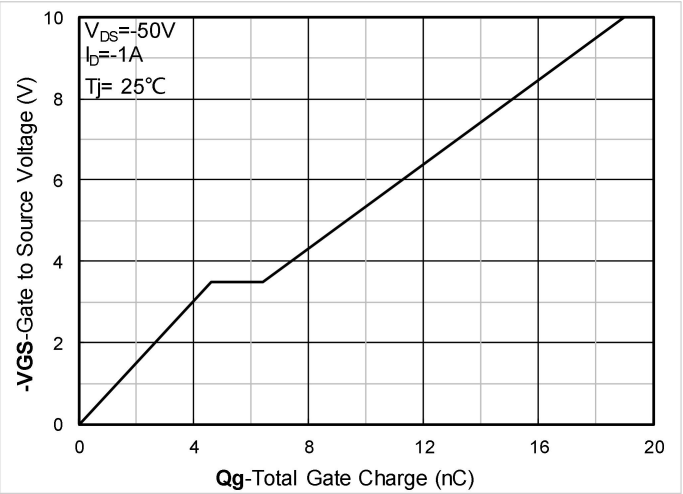


Figure 4. Gate Charge; typical values

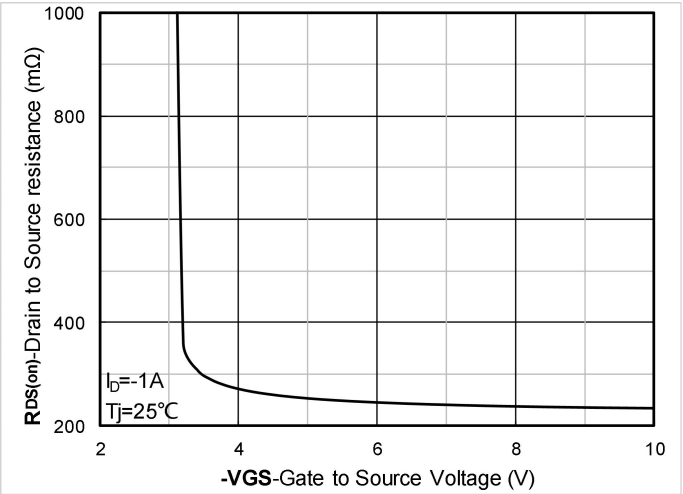


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

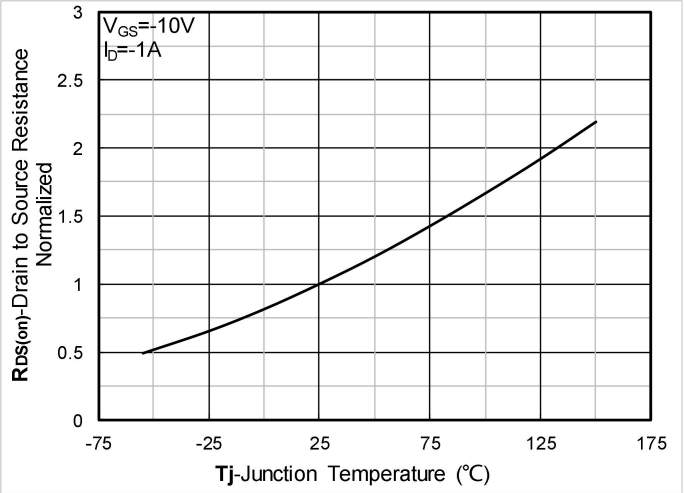


Figure 6. Normalized On-Resistance

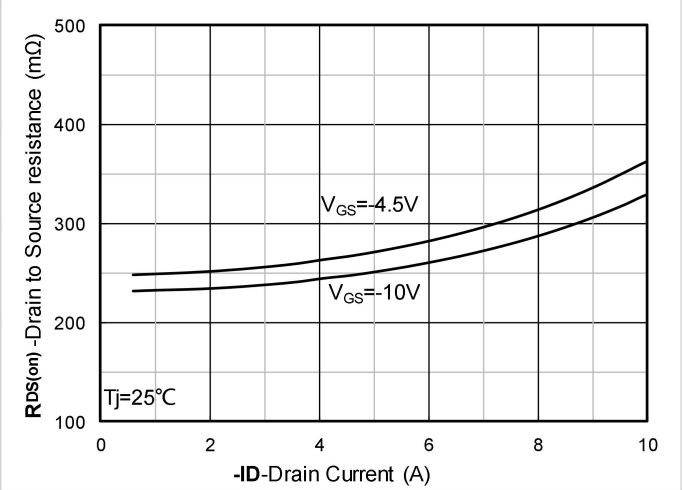


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

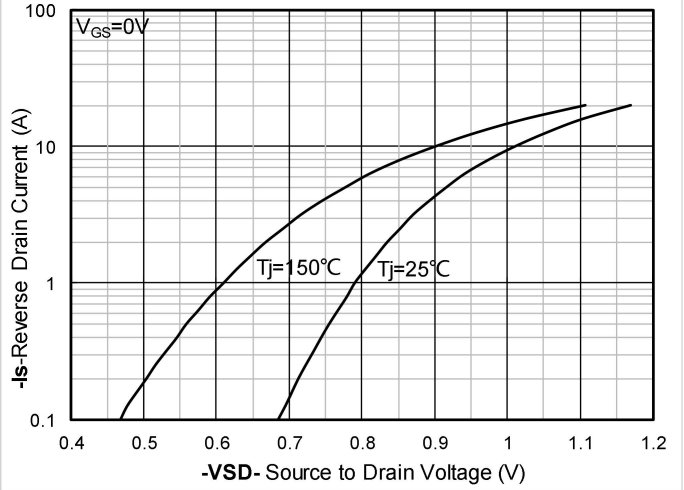


Figure 8. Forward characteristics of reverse diode; typical values

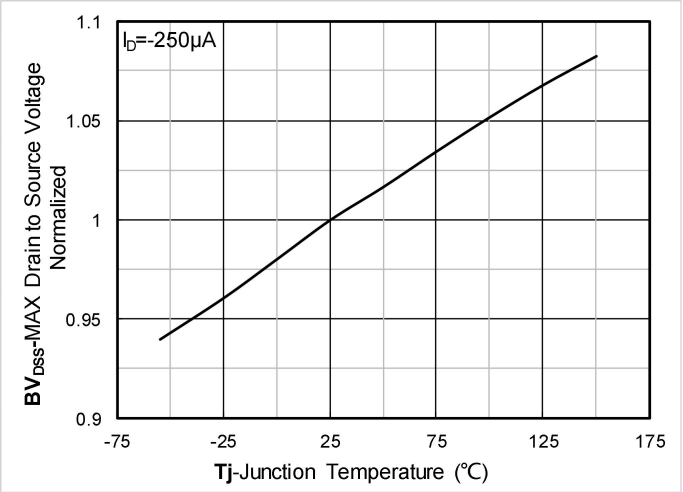


Figure 9. Normalized breakdown voltage

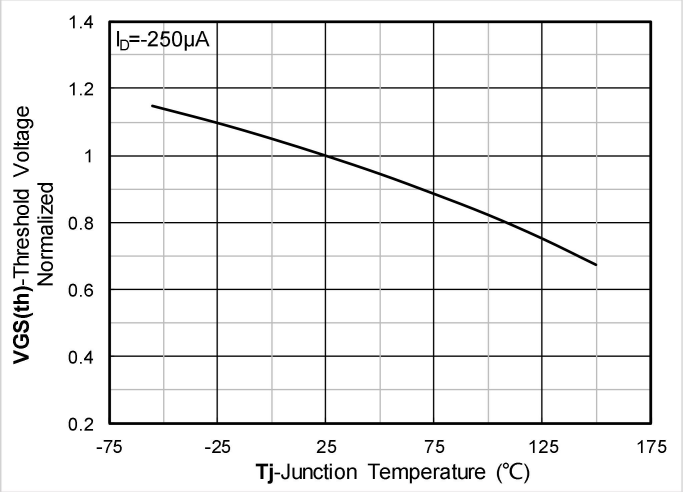


Figure 10. Normalized Threshold voltage

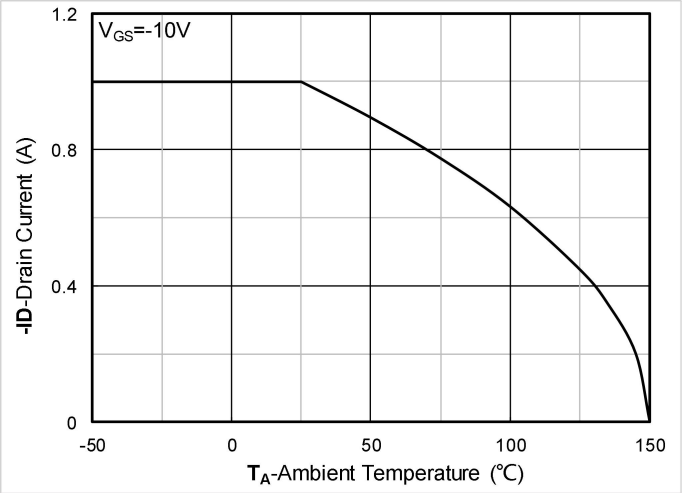


Figure 11. Current dissipation

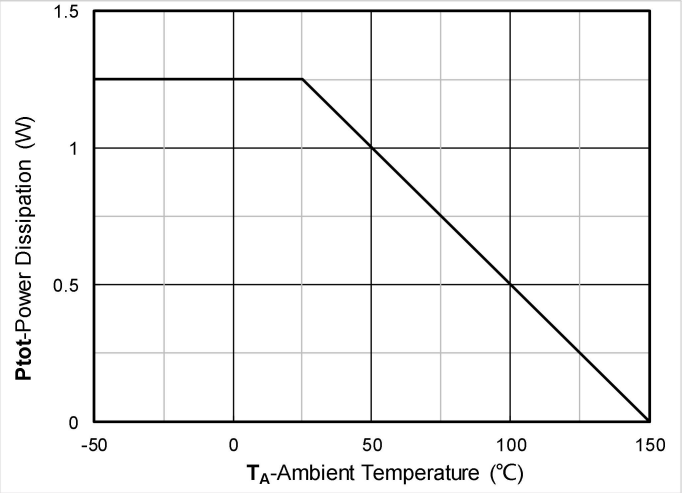


Figure 12. Power dissipation

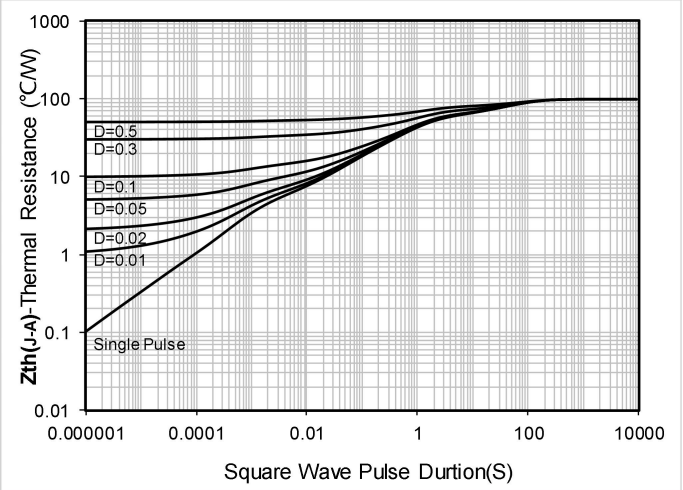


Figure 13. Maximum Transient Thermal Impedance

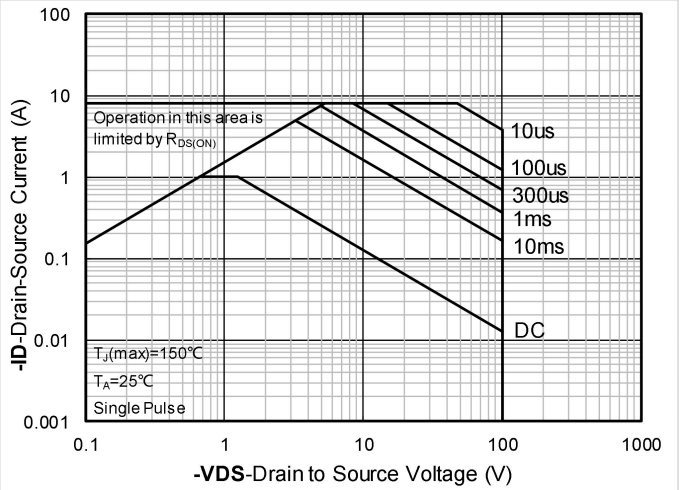
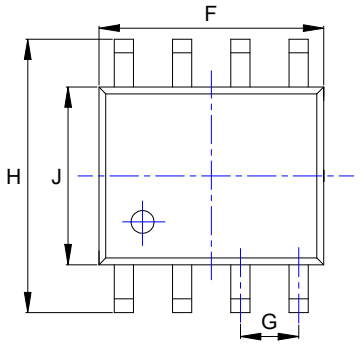
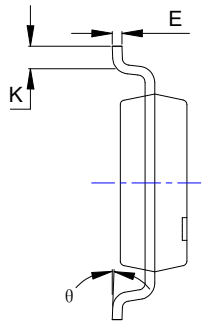


Figure 14. Safe Operation Area

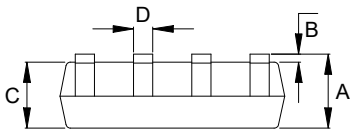
■ SOP-8 Package information



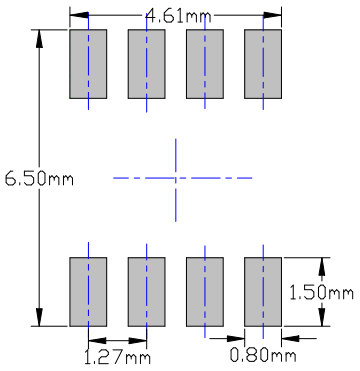
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

Notice

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