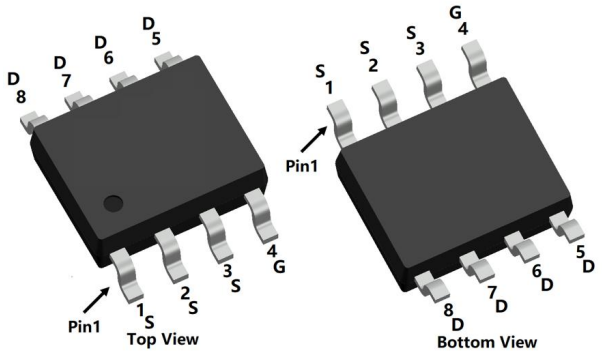
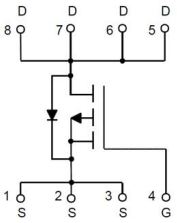
P-Channel Enhancement Mode Field Effect Transistor



SOP-8



Product Summary

- V_{DS} -100V
- I_D -2A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜200mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜246mΩ
- 100% EAS Tested
- ESD Level(HBM) Class 1C

General Description

- Extremely low switching loss
- Excellent stability and uniformity
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power management
- Load switch

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	-100	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=-10V	I_D	-	-2	A
		T_A=100℃,V_{GS}=-10V		-	-1.26	
Pulsed Drain Current	T_A=25℃,t_p≤10μs		I_{DM}	-	-16	
Maximum Body-Diode Continuous Current	T_A=25℃		I_S		-1.5	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=-10V,R_G=25Ω,L=0.5mH,I_{AS}=-10A		EAS	-	25	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	1.78	W
		T_A=100℃		-	0.71	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	150	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	70	℃/W

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
S200P10AJ	F2	S200P10A	4000	8000	64000	13“ reel

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA,Tj=25℃	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V,Tj=25℃	-	-	-1	μA
		V_{DS}=-100V,V_{GS}=0V,Tj=150℃	-	-	-100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA,Tj=25℃	-1	-1.5	-2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V,I_D=-2A,Tj=25℃	-	154	200	mΩ
		V_{GS}=-4.5V,I_D=-1A,Tj=25℃	-	164	246	mΩ
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS}=0V,Tj=25℃	-	-0.77	-1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	20	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-50V,V_{GS}=0V,f=1MHz,Tj=25℃	-	1341	-	pF
Output Capacitance	C_{oss}		-	35	-	
Reverse Transfer Capacitance	C_{rss}		-	28	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-50V,I_D=-2A,Tj=25℃	-	25.5	-	nC
Gate-Source Charge	Q_{gs}		-	2.6	-	
Gate-Drain Charge	Q_{gd}		-	3.1	-	
Reverse Recovery Charge	Q_{rr}	I_F=-2A,di/dt=100A/μs,V_{GS}=0V, V_R=-50V,Tj=25℃	-	32	-	nC
Reverse Recovery Time	t_{rr}		-	24	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DS}=-50V,I_D=-2A,R_{GEN}=3Ω, Tj=25℃	-	5.9	-	ns
Turn-on Rise Time	t_r		-	3.6	-	
Turn-off Delay Time	$t_{D(off)}$		-	140	-	
Turn-off Fall Time	t_f		-	55	-	

Note:

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 80mm*80mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■Typical Electrical and Thermal Characteristics Diagrams

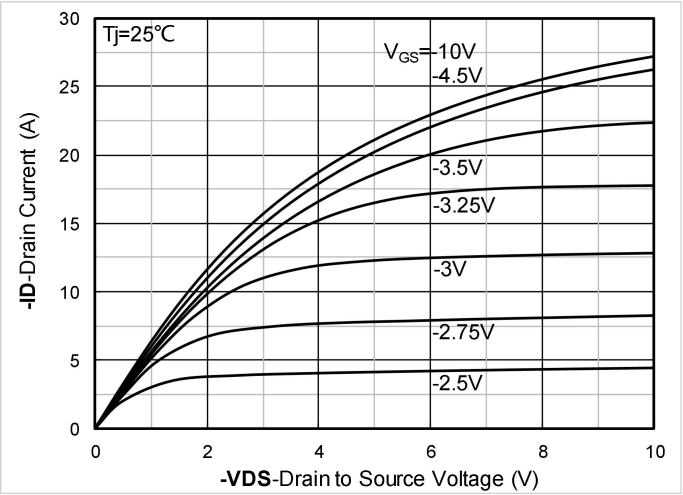


Figure 1. Output Characteristics; typical values

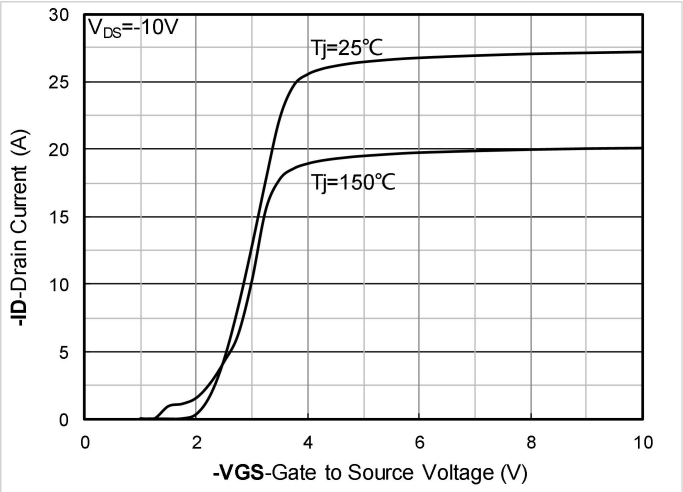


Figure 2. Transfer Characteristics; typical values

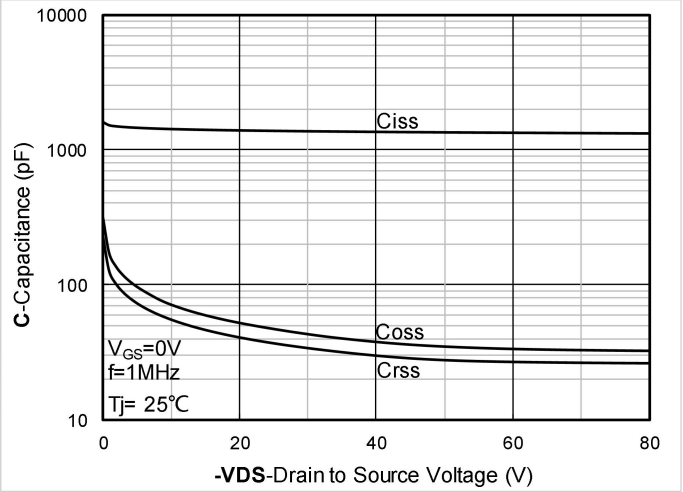


Figure 3. Capacitance Characteristics; typical values

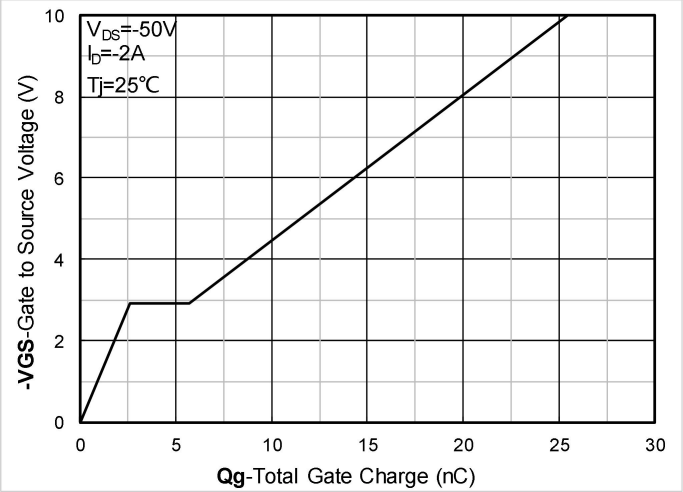


Figure 4. Gate Charge; typical values

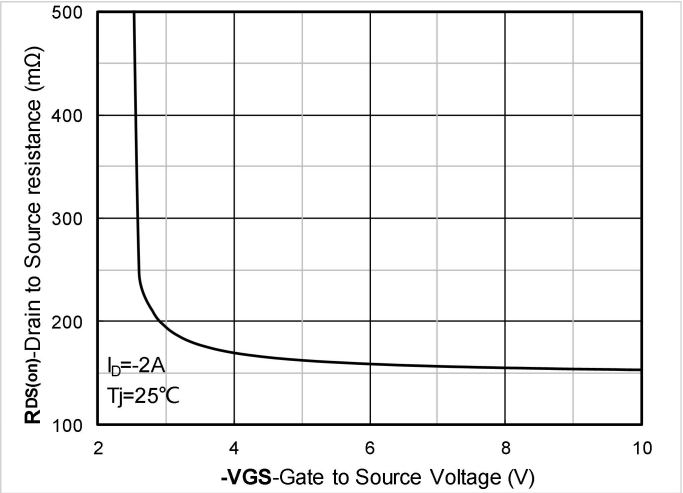


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

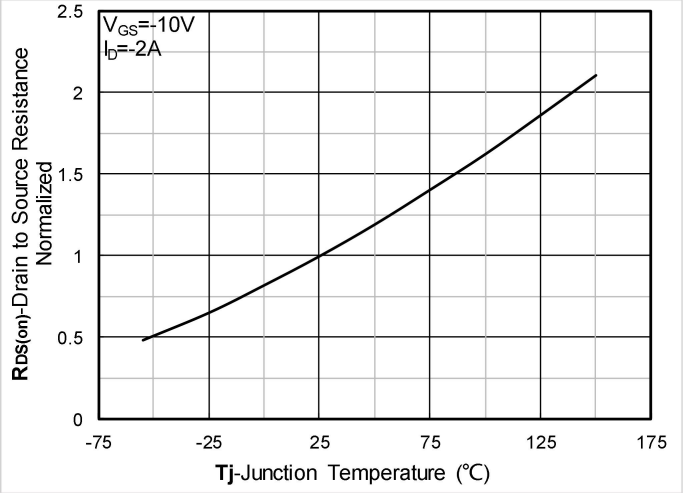


Figure 6. Normalized On-Resistance

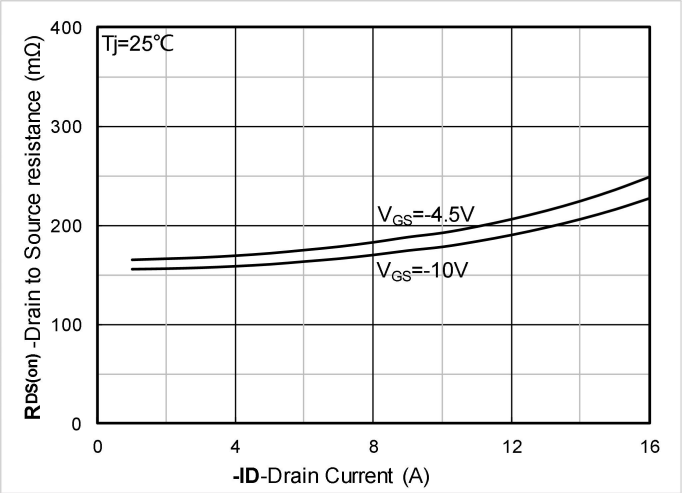


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

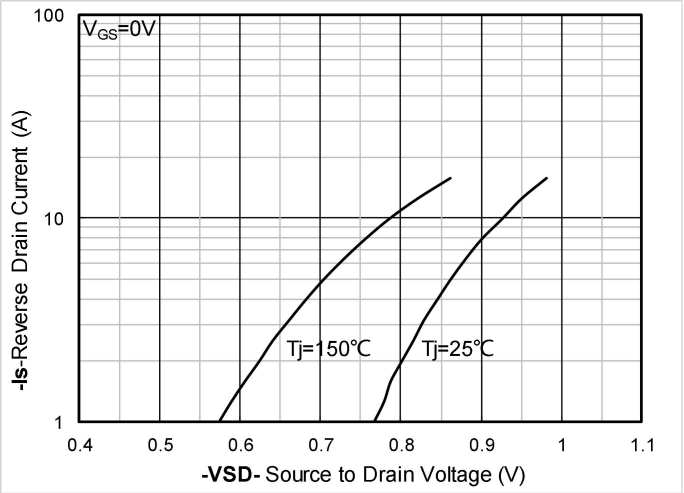


Figure 8. Forward characteristics of reverse diode; typical values

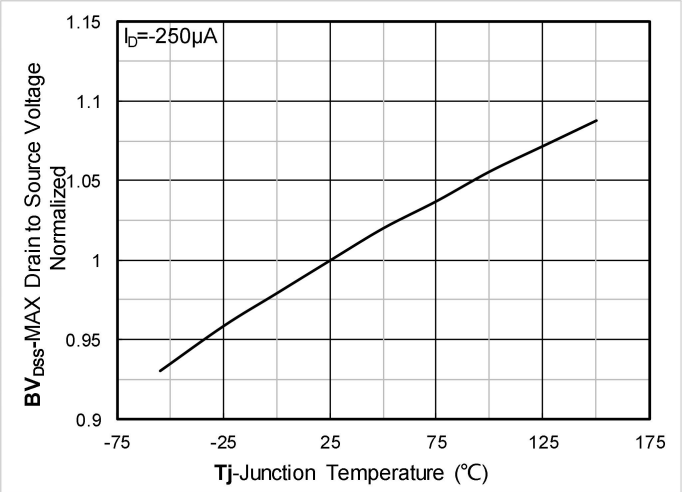


Figure 9. Normalized breakdown voltage

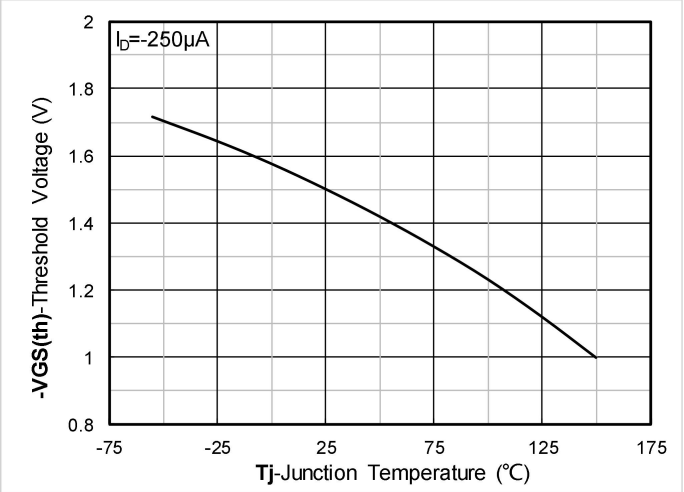


Figure 10. Gate Threshold voltage; typical values

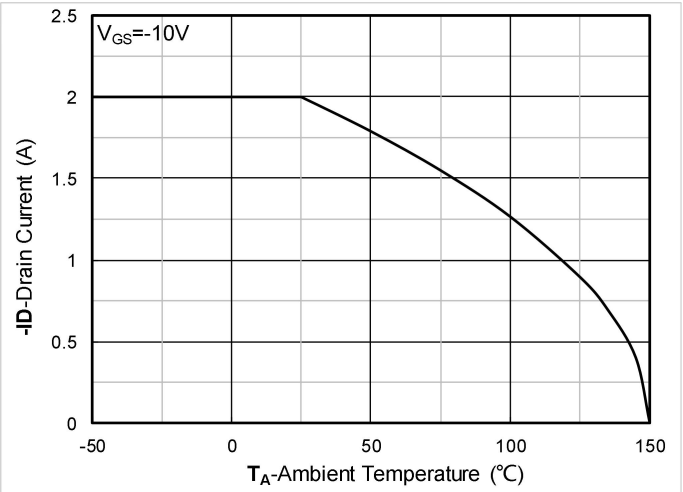


Figure 11. Current dissipation

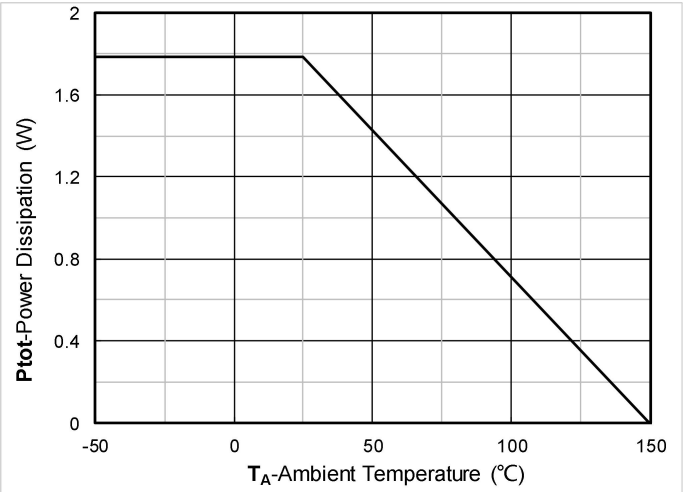


Figure 12. Power dissipation

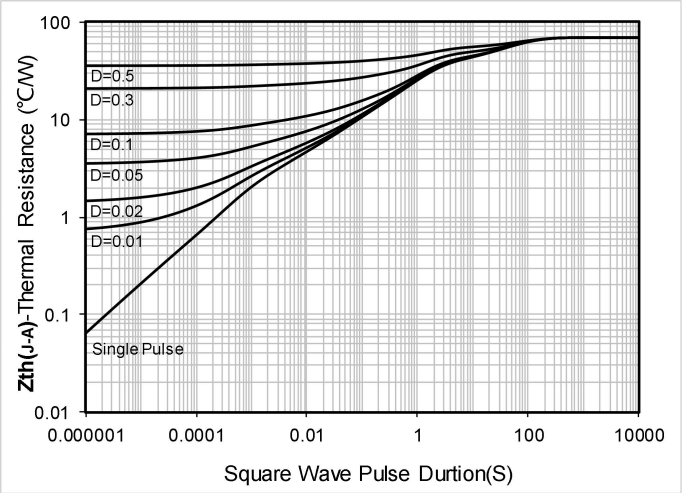


Figure 13. Maximum Transient Thermal Impedance

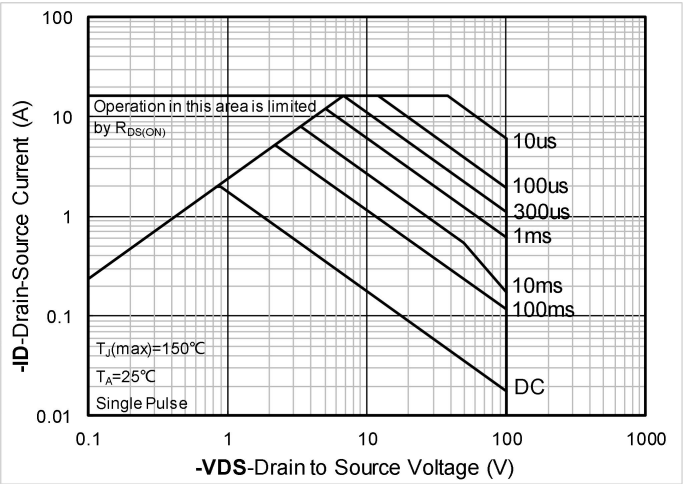
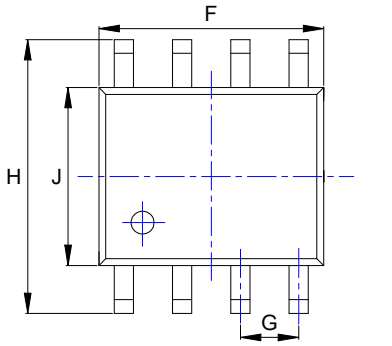
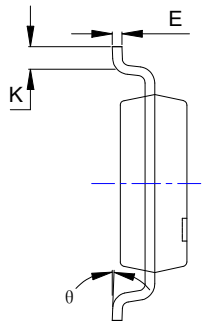


Figure 14. Safe Operation Area

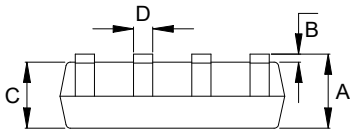
■ SOP-8 Package information



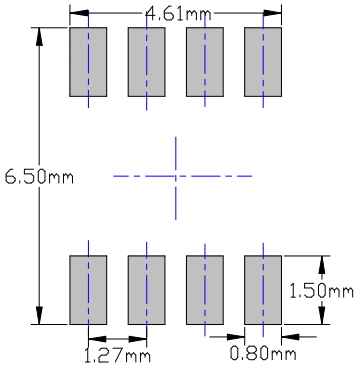
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

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