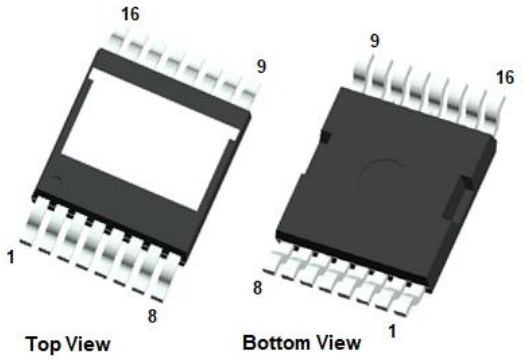
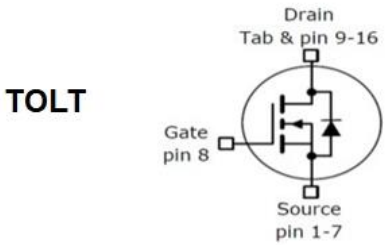
N-Channel Enhancement Mode Field Effect Transistor





Product Summary

- V_{DS} 80V
- I_D 453A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜1.13mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested
- ESD Level(HBM) Class 3B

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- BLDC Motor driver
- Load Switch
- DC-DC convertor
- 48V Port

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	80	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	42.1	A
		T_A=100℃,V_{GS}=10V		-	29.8	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V,Chip limitation		-	453	
		T_C=100℃,V_{GS}=10V		-	320	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	1812	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		360	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=10V, R_G=25Ω, L=1mH, I_{AS}=56A		EAS	-	1568	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	4	W
		T_A=100℃		-	2	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	468	
		T_C=100℃		-	234	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	175	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	37	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.32	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
TL1D1G08H	F1	TL1D1G08H	1200	1200	6000	13” reel

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=1mA,Tj=25℃	80	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=80V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2.2	3	3.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=50A,Tj=25℃	-	0.86	1.13	mΩ
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V,Tj=25℃	-	0.78	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	3.2	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=40V,V_{GS}=0V,f=1MHz,Tj=25℃	-	12790	-	pF
Output Capacitance	C_{oss}		-	3130	-	
Reverse Transfer Capacitance	C_{rss}		-	106	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=40V,I_D=50A,Tj=25℃	-	219	-	nC
Gate-Source Charge	Q_{gs}		-	55	-	
Gate-Drain Charge	Q_{gd}		-	69	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs,V_{GS}=0V,V_R=40V, Tj=25℃	-	158	-	nC
Reverse Recovery Time	t_{rr}		-	84	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=40V,I_D=50A,R_{GEN}=3Ω, Tj=25℃	-	23.5	-	ns
Turn-on Rise Time	t_r		-	152	-	
Turn-off Delay Time	$t_{D(off)}$		-	110	-	
Turn-off Fall Time	t_f		-	120	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

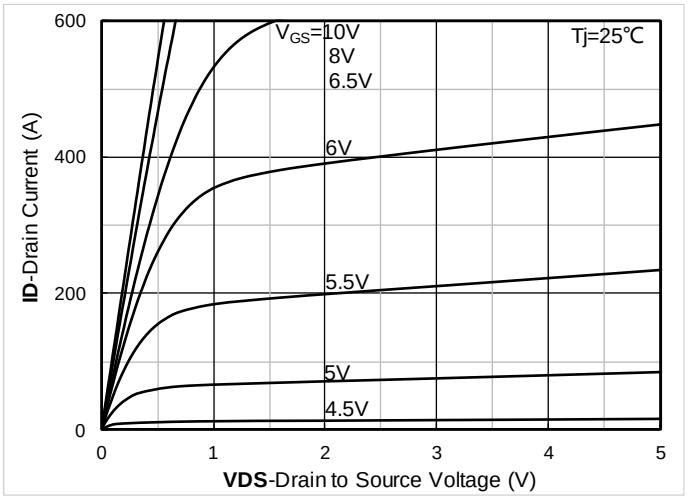


Figure 1. Output Characteristics; typical values

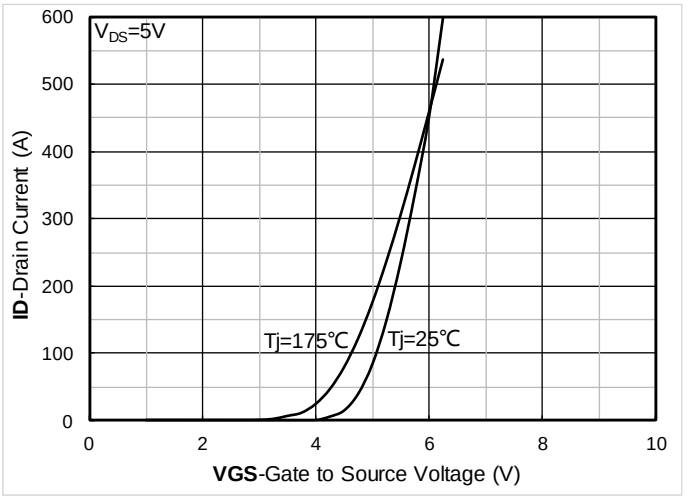


Figure 2. Transfer Characteristics; typical values

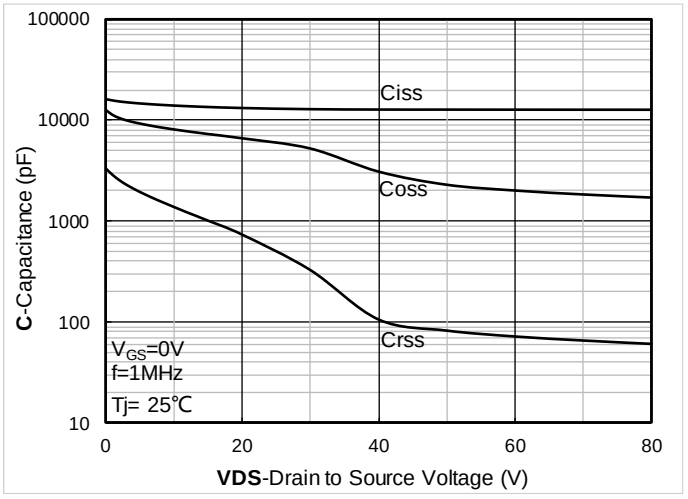


Figure 3. Capacitance Characteristics; typical values

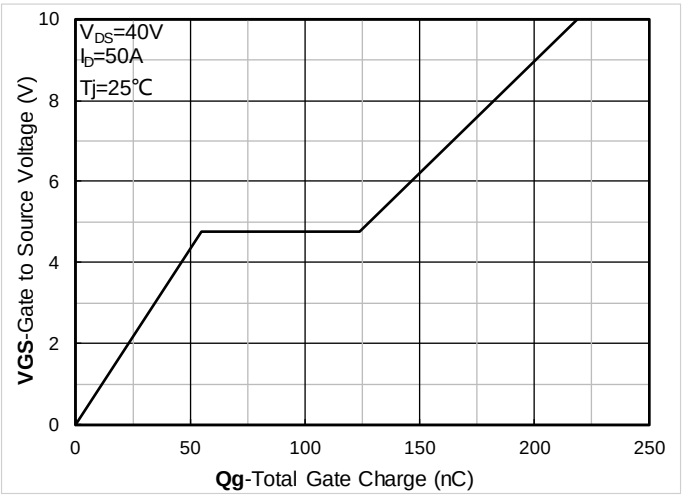


Figure 4. Gate Charge; typical values

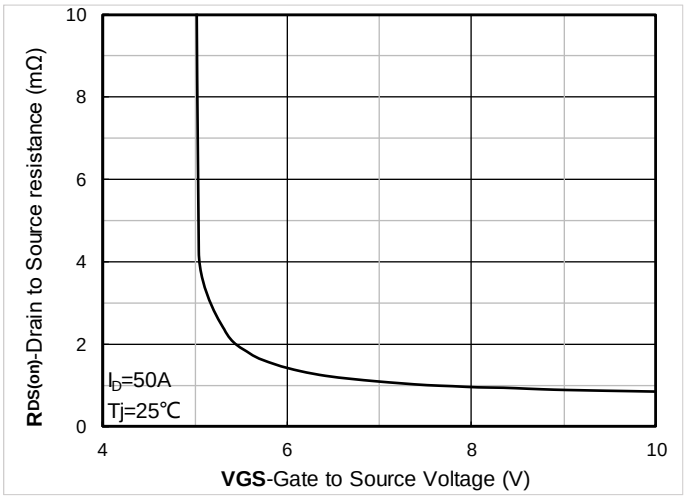


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

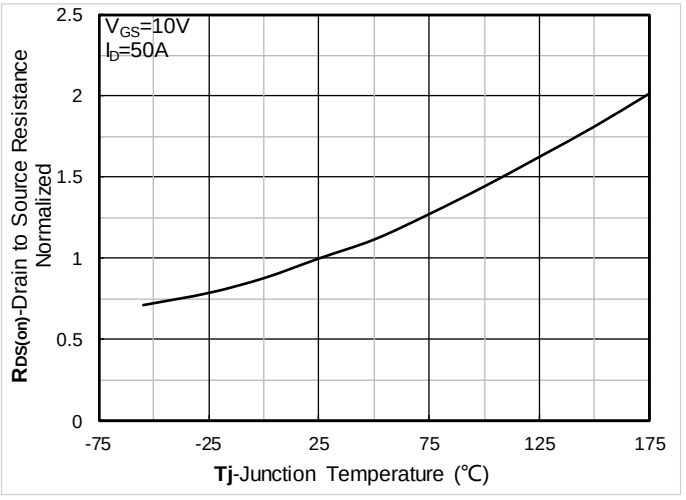


Figure 6. Normalized On-Resistance

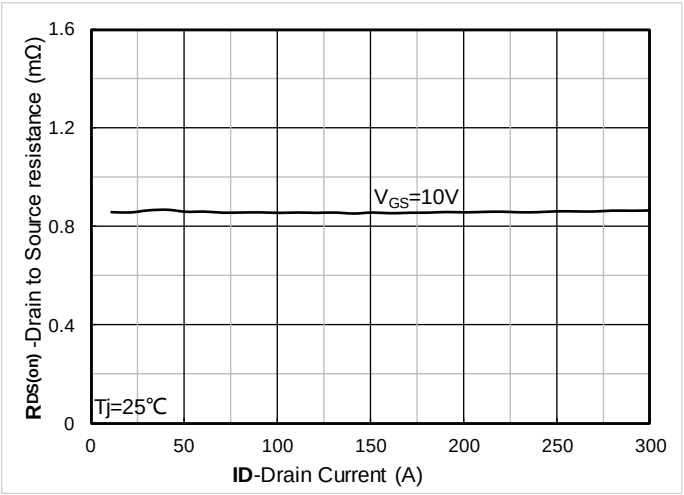


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

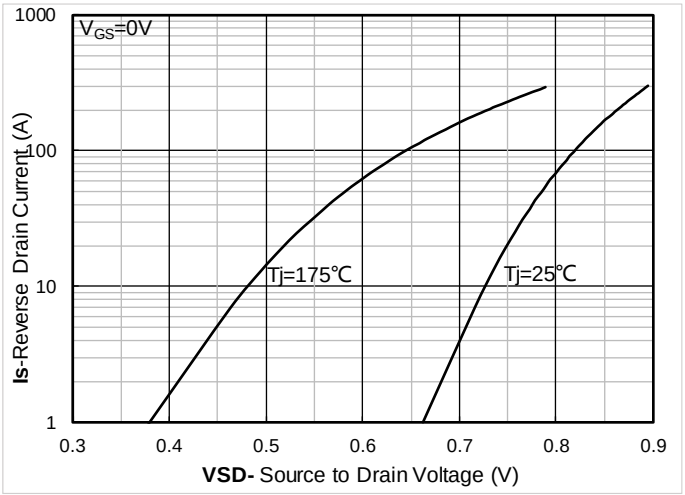


Figure 8. Forward characteristics of reverse diode; typical values

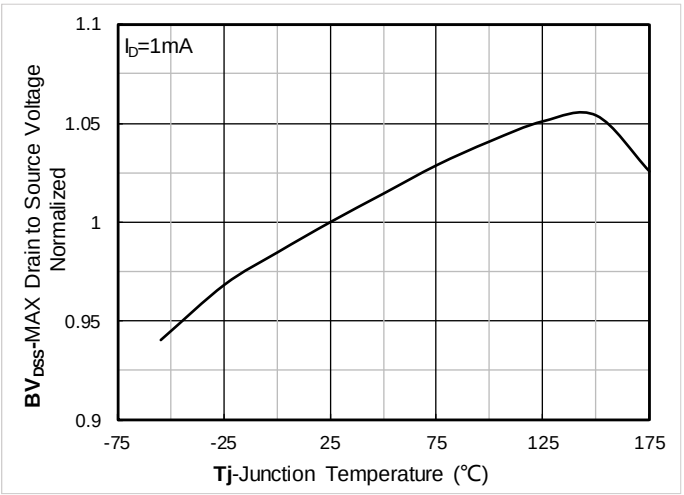


Figure 9. Normalized breakdown voltage

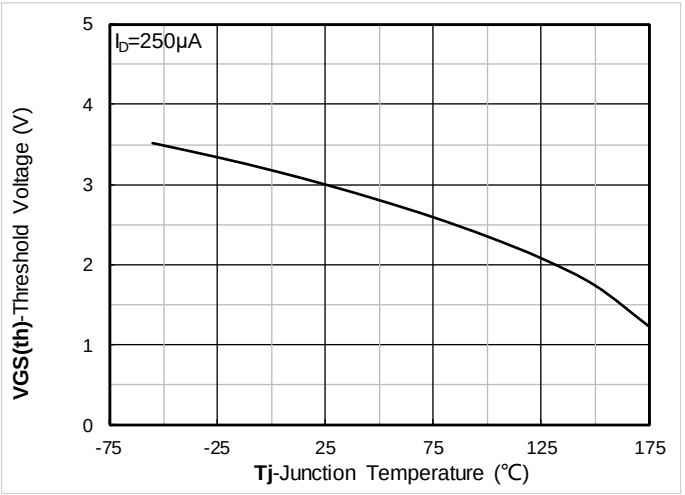


Figure 10. Gate Threshold voltage; typical values

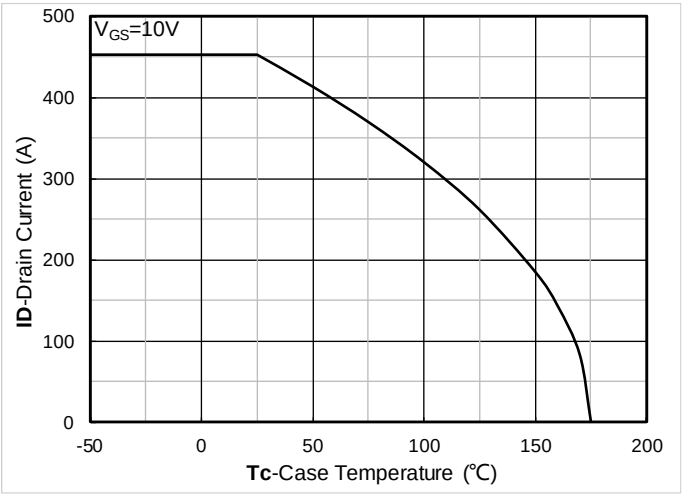


Figure 11. Current dissipation

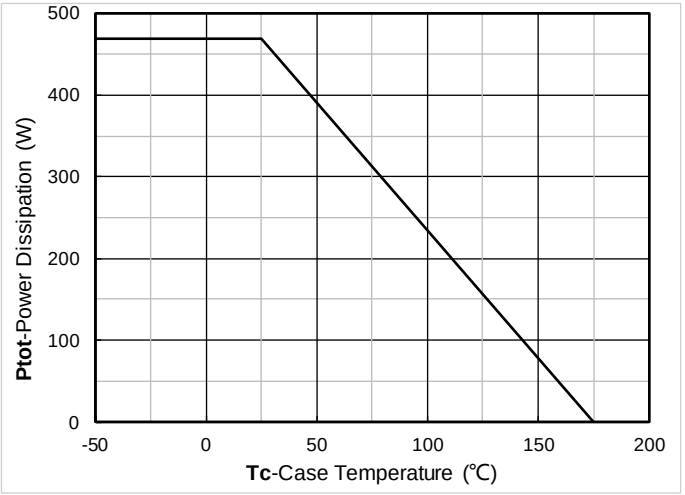


Figure 12. Power dissipation

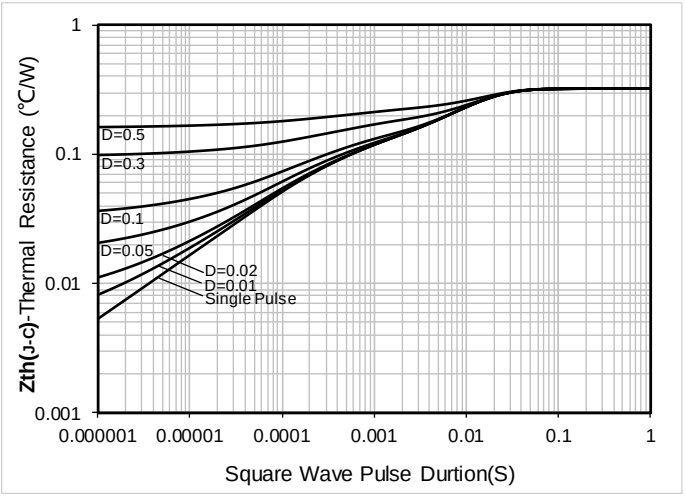


Figure 13. Maximum Transient Thermal Impedance

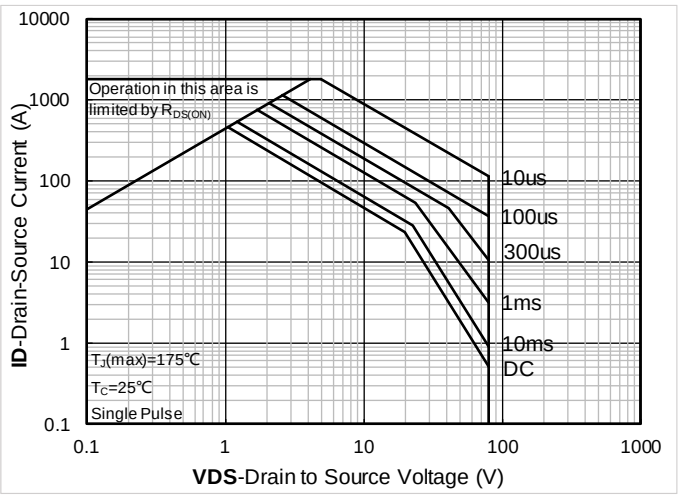
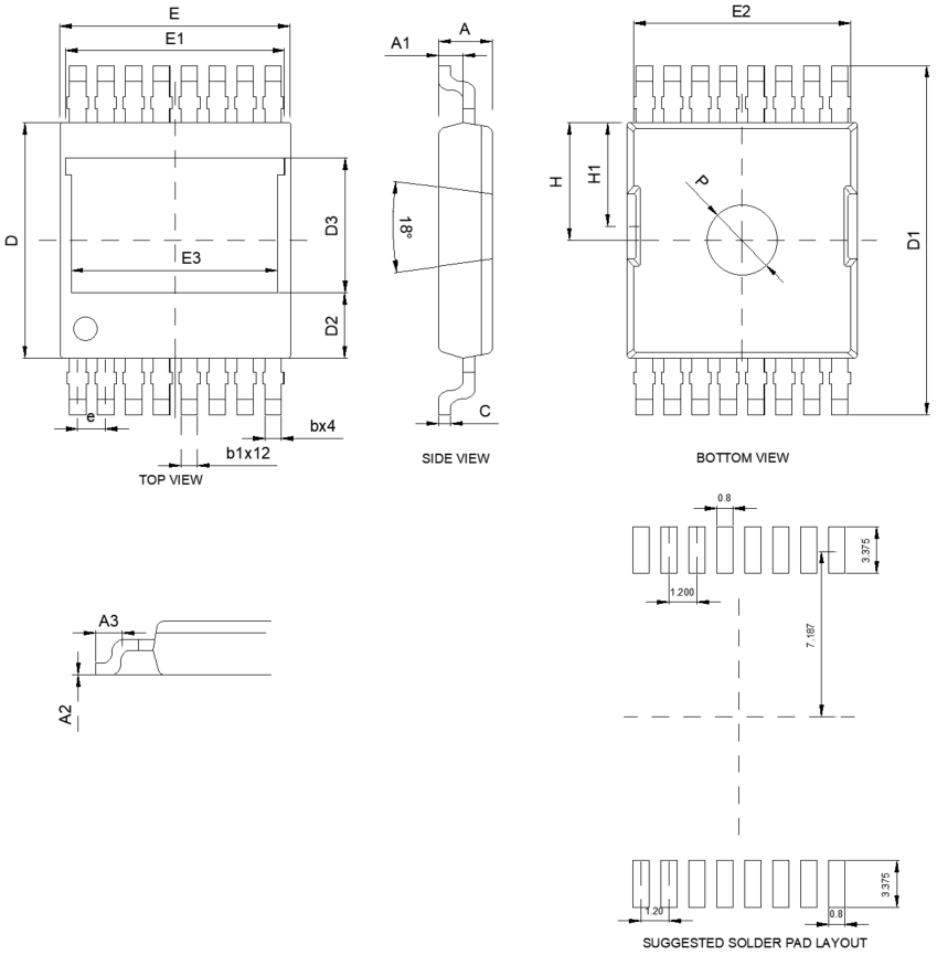


Figure 14. Safe Operation Area

■ TOLT Package Information



DIMENSIONS			
SYMBOL	Millimeter		
	MIN	NOM	MAX
A	2.25	2.30	2.35
A1	1.00	1.04	1.08
A2	0.01	0.08	0.16
A3		1.50REF	
b	0.70	0.75	0.80
b1	0.60	0.70	0.80
c	0.40	0.50	0.60
D	10.00	10.10	10.30
D1	14.80	15.00	15.20
D2	2.60	2.80	3.00
D3		5.77REF	
E	9.70	9.90	10.10
E1		9.46REF	
E2		9.25REF	
E3		8.70REF	
e	1.18	1.20	1.22
H	5.00	5.20	5.40
H1	4.40	4.60	4.80
L	2.40	2.45	2.50
P	2.80	3.00	3.20

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY

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