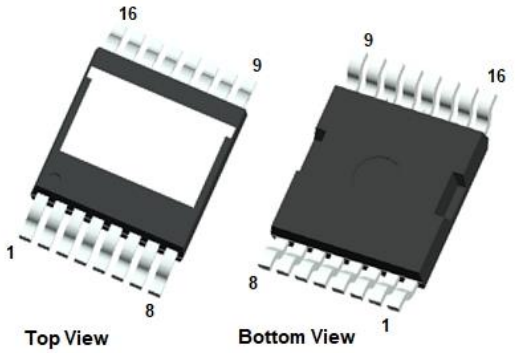
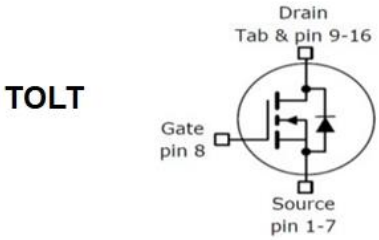
N-Channel Enhancement Mode Field Effect Transistor





Product Summary

- V_{DS} 100V
- I_D 340A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜1.7mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested
- ESD Level(HBM) H3A

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High power inverter system
- BMS appliances

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	100	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=10V	I_D	-	34	A
		T_A=100℃,V_{GS}=10V		-	24	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=10V,Chip limitation		-	340	
		T_C=100℃,V_{GS}=10V		-	240	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	1360	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		285	
Avalanche energy (non-repetitive)	T_J=25℃,V_G=10V, R_G=25Ω, L=5mH, I_{AS}=33A		EAS	-	2722.5	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	4.1	W
		T_A=100℃		-	2	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	416	
		T_C=100℃		-	208	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	175	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	36	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.36	

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=1mA,Tj=25℃	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=80V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2	2.6	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=20A,Tj=25℃	-	1.2	1.7	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V,Tj=25℃	-	0.75	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	1.45	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHz,Tj=25℃	-	10700	-	pF
Output Capacitance	C_{oss}		-	2010	-	
Reverse Transfer Capacitance	C_{rss}		-	35	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=30A,Tj=25℃	-	166	-	nC
Gate-Source Charge	Q_{gs}		-	34	-	
Gate-Drain Charge	Q_{gd}		-	49	-	
Reverse Recovery Charge	Q_{rr}	I_F=30A,di/dt=100A/μs,V_{GS}=0V,V_R=50V, Tj=25℃	-	167	-	nC
Reverse Recovery Time	t_{rr}		-	92	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=50V,I_D=30A,R_{GEN}=4.5Ω, Tj=25℃	-	30	-	ns
Turn-on Rise Time	t_r		-	65	-	
Turn-off Delay Time	$t_{D(off)}$		-	121	-	
Turn-off Fall Time	t_f		-	107	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with T_A=25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

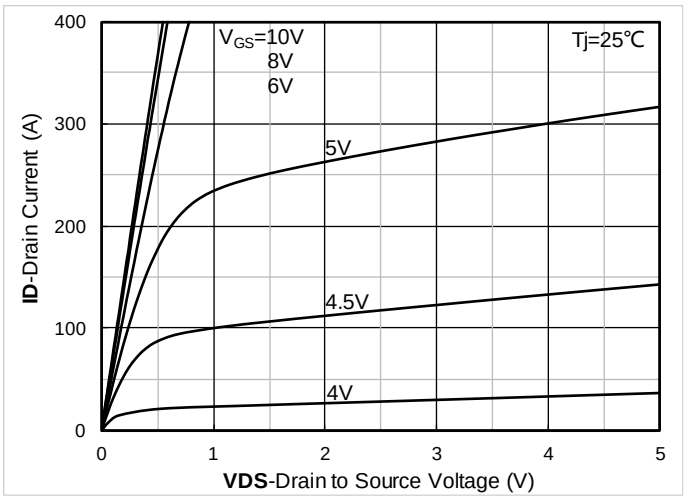


Figure 1. Output Characteristics

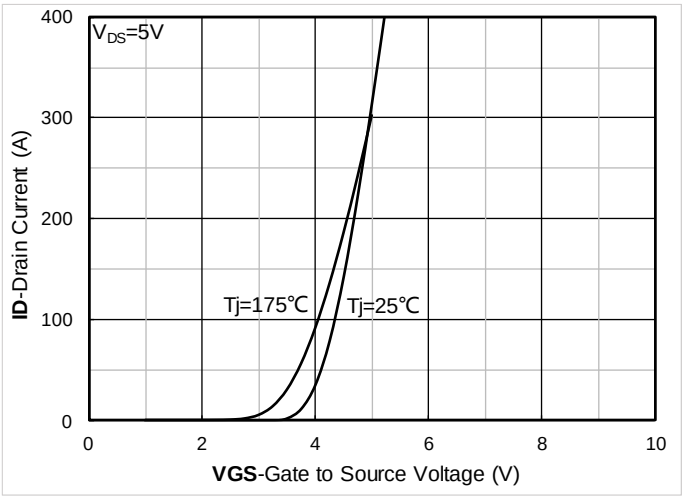


Figure 2. Transfer Characteristics

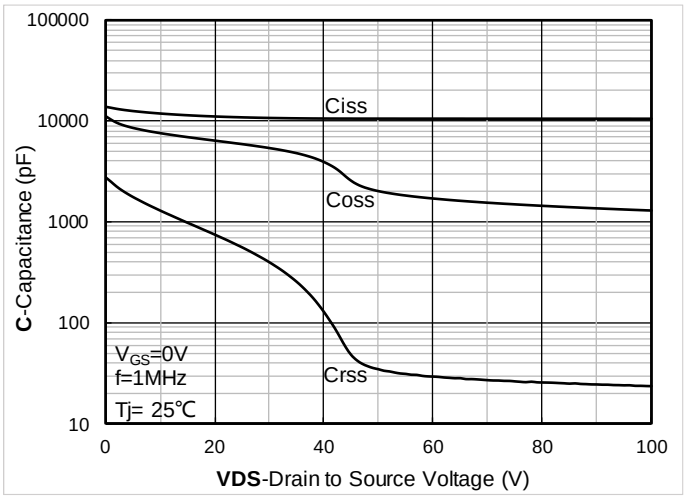


Figure 3. Capacitance Characteristics

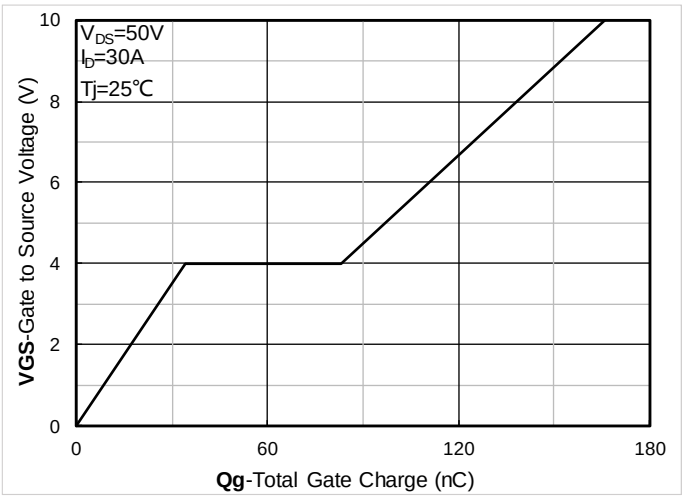


Figure 4. Gate Charge

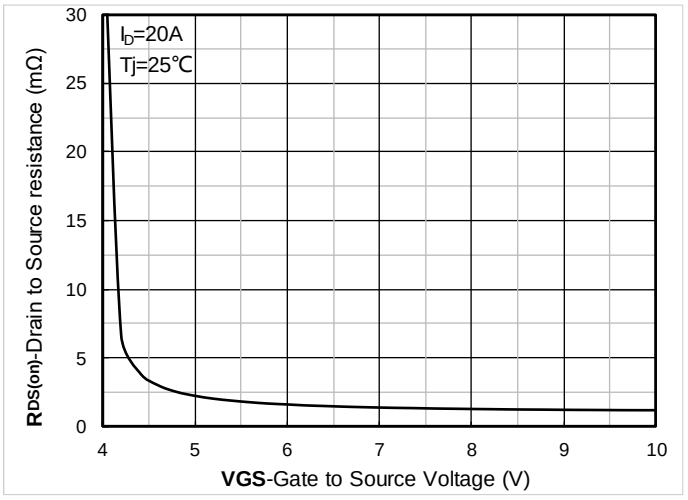


Figure 5. On-Resistance vs. Gate to Source Voltage

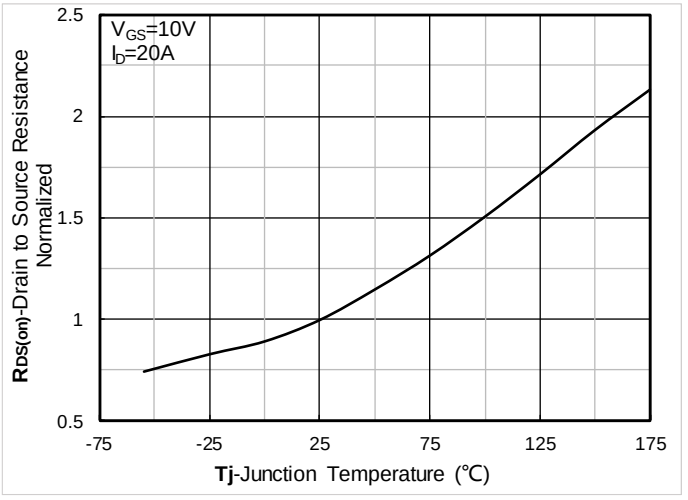


Figure 6. Normalized On-Resistance

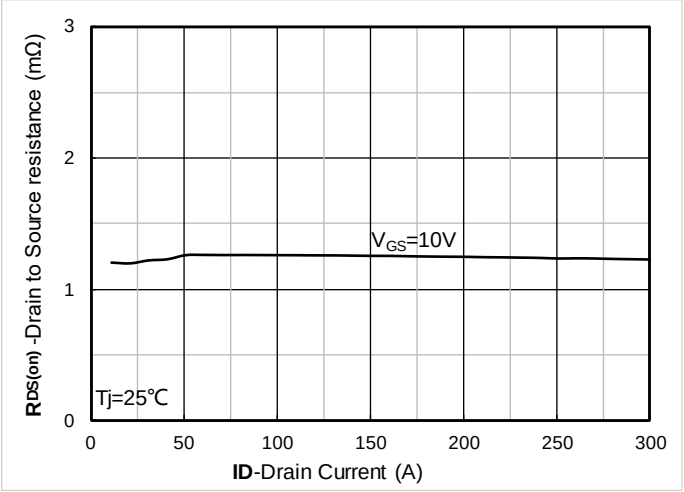


Figure 7. $R_{DS(on)}$ vs. Drain Current

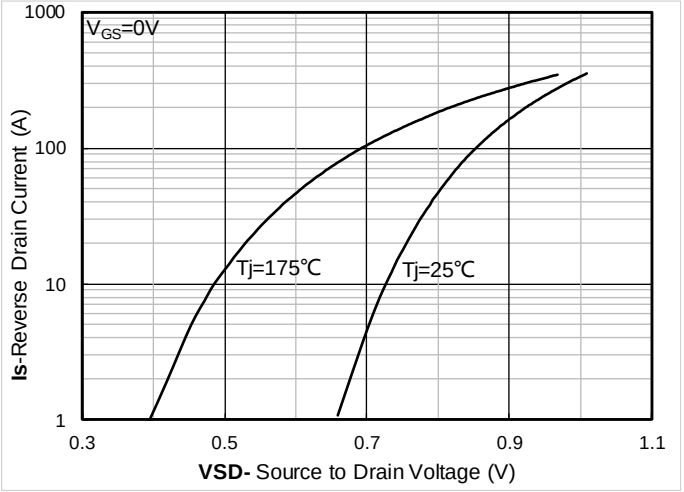


Figure 8. Forward characteristics of reverse diode

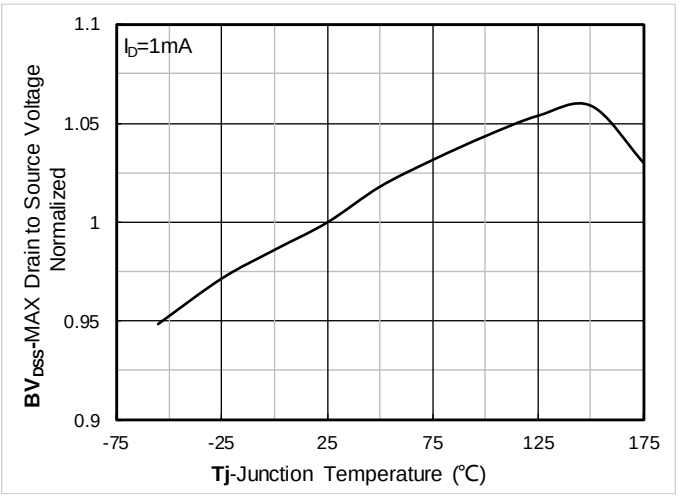


Figure 9. Normalized breakdown voltage

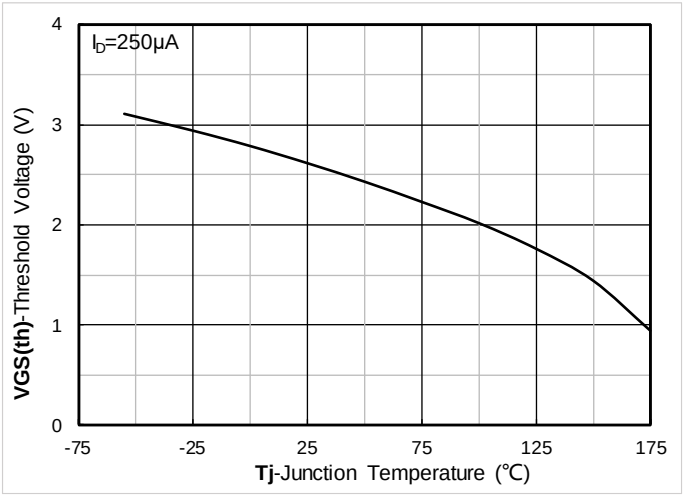


Figure 10. Gate Threshold voltage; typical values

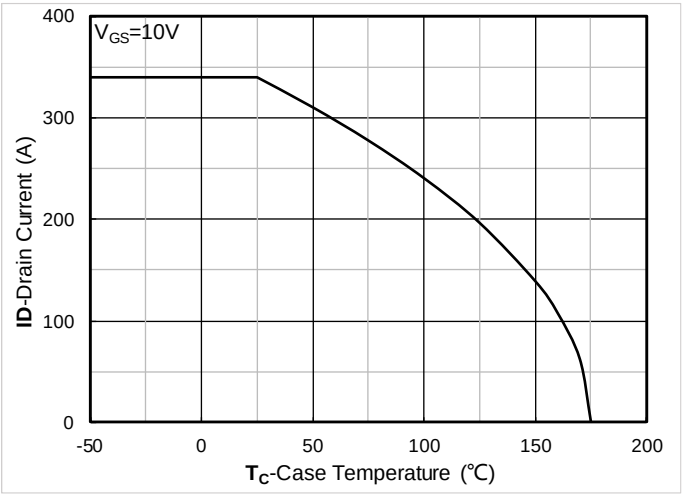


Figure 11. Current dissipation

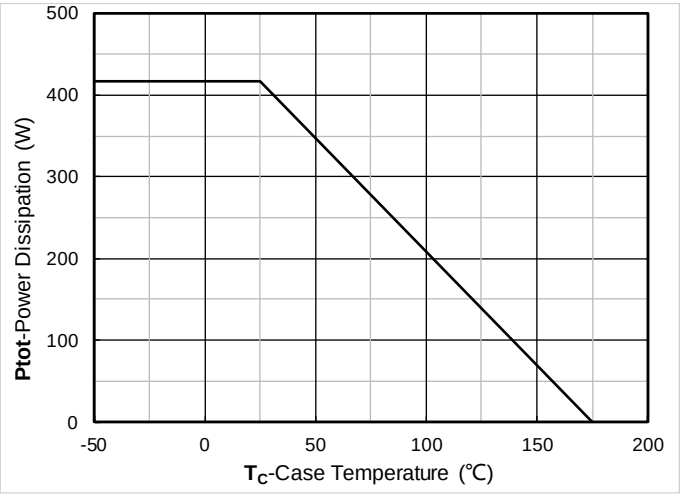


Figure 12. Power dissipation

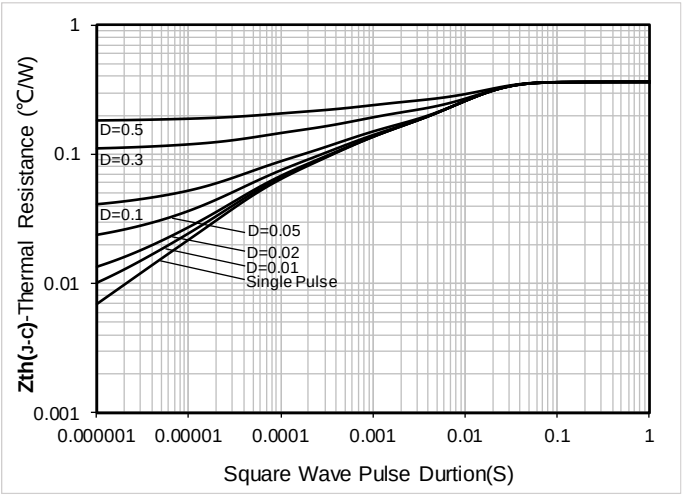


Figure 13. Maximum Transient Thermal Impedance

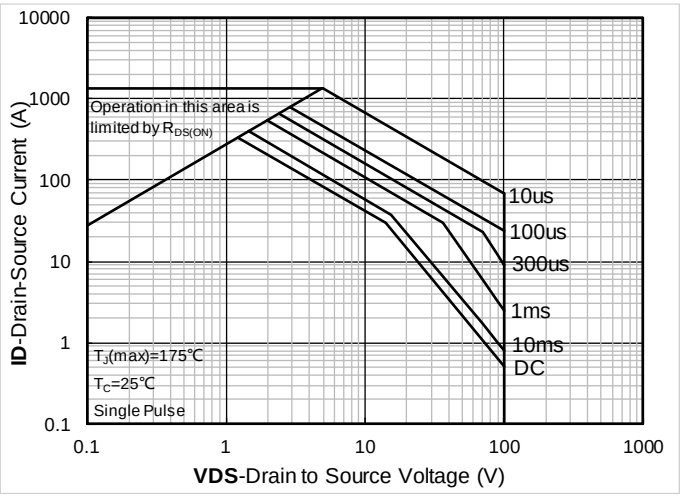
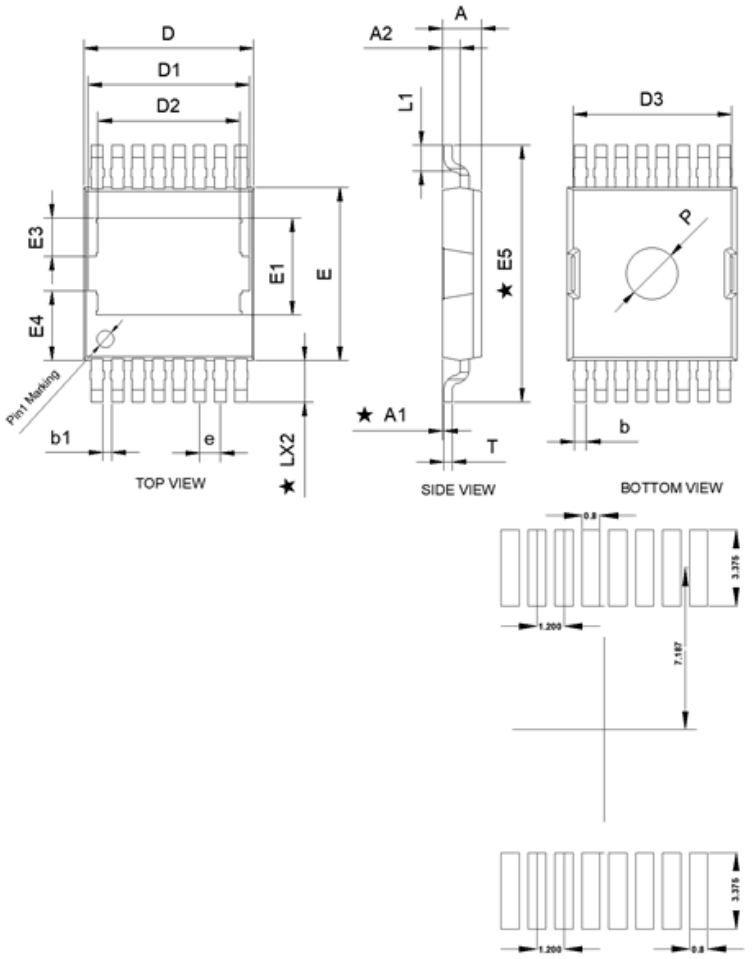


Figure 14. Safe Operation Area

■ TOLT Package information



SYMBOY	MILLMETER		
	MIN	NOR	MAX
A	2.25	2.30	2.35
A1	0.01	0.08	0.16
A2	0.99	1.04	1.09
b	0.60	0.70	0.80
b1	0.40	0.50	0.60
D	9.70	9.90	10.10
D1	9.36	9.46	9.56
D2	8.20	8.30	8.40
D3	9.17	9.27	9.37
e	1.20BSC		
E	10.00	10.10	10.30
E1	5.47	5.67	5.87
E2	1.90	2.00	2.10
E3	2.05	2.25	2.45
E4	3.90	4.05	4.20
E5	14.80	15.00	15.20
L	2.20	2.45	2.70
L1	1.51REF		
T	0.458	0.508	0.558
P	2.80	3.00	3.20

Note:
1. Controlling dimension:in millimeters.
2. General tolerance:±0.10mm.
3. The pad layout is for reference purposes only.
4. ★It is the key size.

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