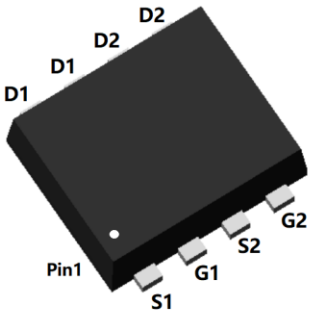
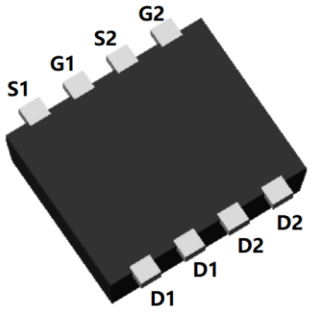
N-Channel and P-Channel Complementary MOSFET

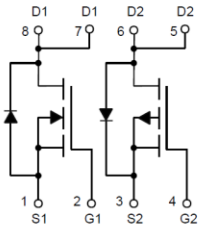


Top View



Bottom View

PDFN3030-8L



Product Summary

NMOS

- V_{DS} 30V
- I_D 8A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜26mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜40mΩ

PMOS

- V_{DS} -30V
- I_D -6A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜43mΩ
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜70mΩ

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation

Applications

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	NMOS	PMOS	Unit
Drain-source Voltage		V_{DS}	30	-30	V
Gate-source Voltage		V_{GS}	±20	±20	V
Drain Current	T_A=25℃@t≤1s	I_D	8	-6	A
	T_A=25℃@Steady-State		6	-4	
	T_A=100℃@Steady-State		3.8	-2.5	
Pulsed Drain Current [A]		I_{DM}	35	-30	A
Total Power Dissipation [B]	T_A=25℃@Steady-State	P_D	1.25	1.25	W
	T_A=100℃@Steady-State		0.5	0.5	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	-55～+150	℃

■Thermal resistance

Parameter		Symbol	NMOS		PMOS		Units
			Typ	Max	Typ	Max	
Thermal Resistance Junction-to-Ambient [C]	t≤1s	$R_{\theta JA}$	30	37.5	33	41	℃/W
	Steady-State		80	100	80	100	℃/W

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
U4606A	F1	Q4606A	3000	30000	120000	7“ reel

■ NMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	-	-	1	μA
		V_{DS}=30V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.5	2.2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=6A	-	20	26	mΩ
		V_{GS}=4.5V, I_D=4A	-	30	40	
Diode Forward Voltage	V_{SD}	I_S=6A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	2.5	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	6	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz	-	380	-	pF
Output Capacitance	C_{oss}		-	80	-	
Reverse Transfer Capacitance	C_{rss}		-	60	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=15V, I_D=6A	-	9	-	nC
Gate-Source Charge	Q_{gs}		-	2	-	
Gate-Drain Charge	Q_{gd}		-	2	-	
Reverse Recovery Charge	Q_{rr}	I_F=6A, di/dt=100A/us	-	1	-	nC
Reverse Recovery Time	t_{rr}		-	7	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=15V, I_D=6A R_{GEN}=3Ω	-	6	-	ns
Turn-on Rise Time	t_r		-	41	-	
Turn-off Delay Time	$t_{D(off)}$		-	11	-	
Turn-off fall Time	t_f		-	34	-	

■ PMOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V	-	-	-1	μA
		V_{DS}=-30V, V_{GS}=0V, Tj=150℃	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1	-1.5	-2.4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-4A	-	33	43	mΩ
		V_{GS}=-4.5V, I_D=-4A	-	50	70	
Diode Forward Voltage	V_{SD}	I_S=-4A, V_{GS}=0V	-	-	-1.2	V
Gate resistance	R_G	f=1MHz	-	15	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-4	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHz	-	490	-	pF
Output Capacitance	C_{oss}		-	75	-	
Reverse Transfer Capacitance	C_{rss}		-	60	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-15V, I_D=-4A	-	9	-	nC
Gate-Source Charge	Q_{gs}		-	1.5	-	
Gate-Drain Charge	Q_{gd}		-	2.3	-	
Reverse Recovery Charge	Q_{rr}	I_F=-4A, di/dt=100A/us	-	12	-	nC
Reverse Recovery Time	t_{rr}		-	32	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DD}=-15V, ID=-4A R_{GEN}=2.5Ω	-	9	-	ns
Turn-on Rise Time	t_r		-	3	-	
Turn-off Delay Time	$t_{D(off)}$		-	29	-	
Turn-off fall Time	t_f		-	15	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. P_d is based on max. junction temperature, using junction-case thermal resistance.
C. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■ NMOS Typical Electrical and Thermal Characteristics Diagrams

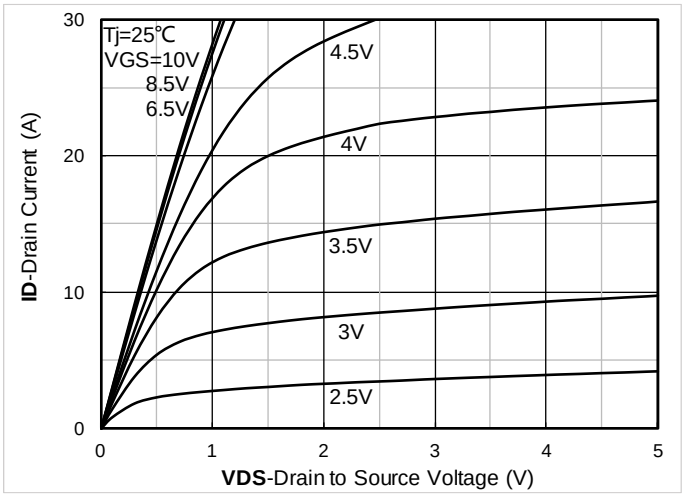


Figure 1. Output Characteristics

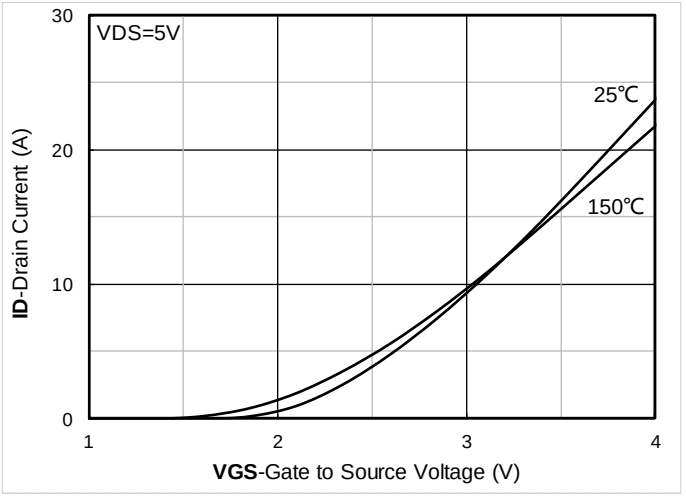


Figure 2. Transfer Characteristics

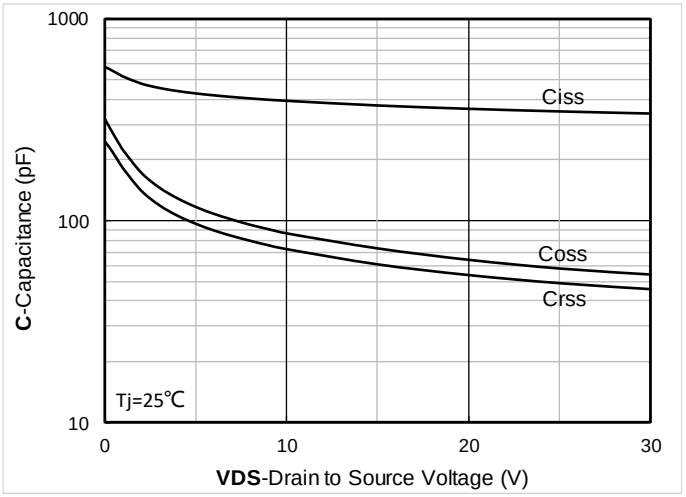


Figure 3. Capacitance Characteristics

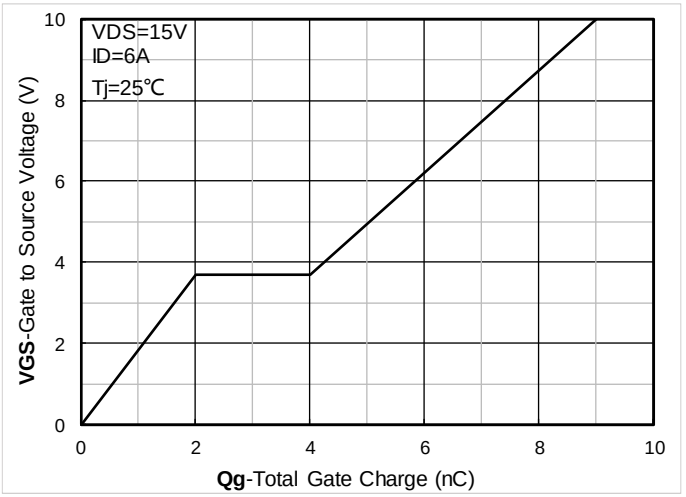


Figure 4. Gate Charge

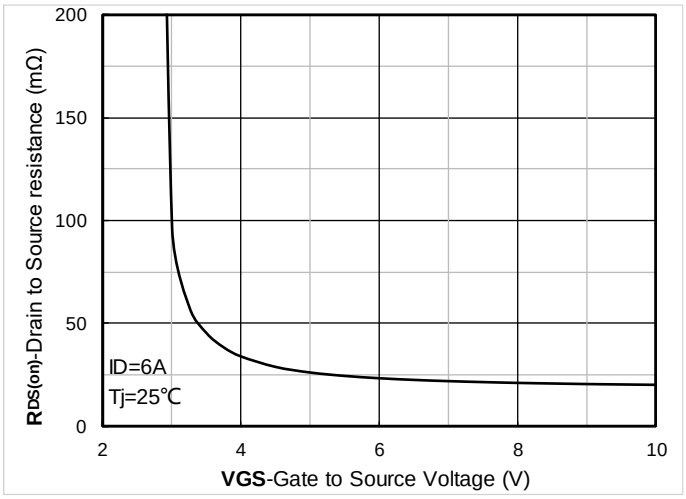


Figure 5. On-Resistance vs Gate to Source Voltage

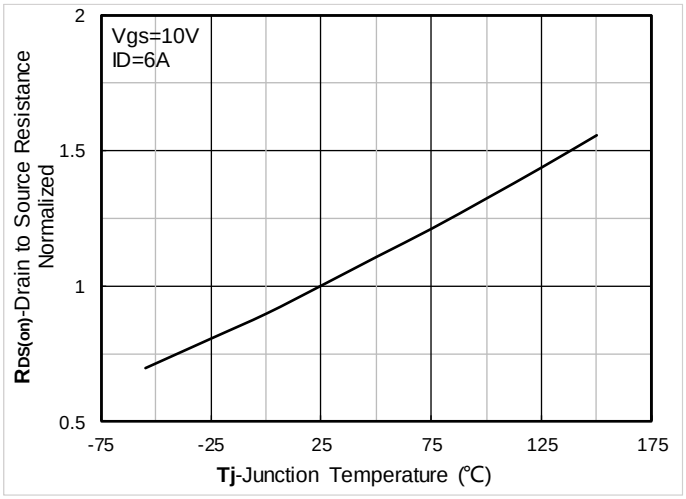


Figure 6. Normalized On-Resistan

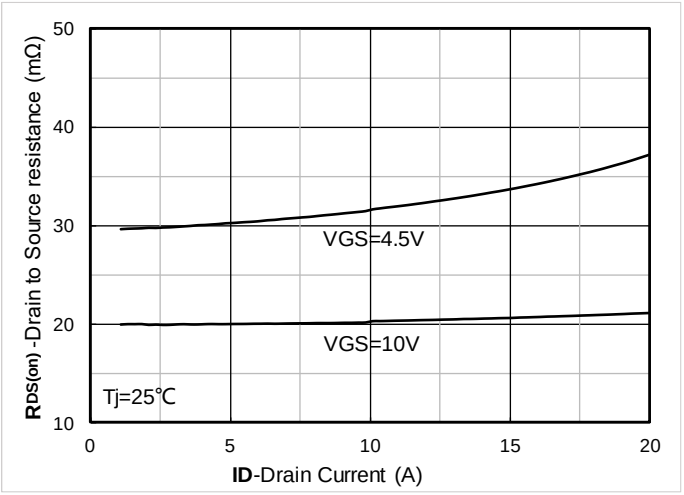


Figure 7. $R_{DS(on)}$ VS Drain Current

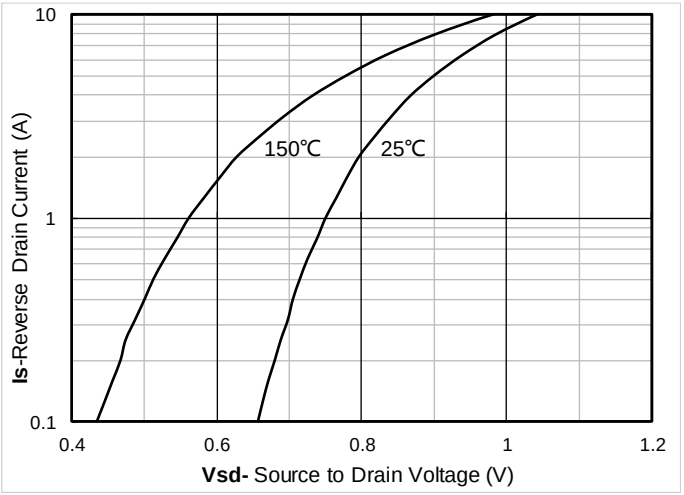


Figure 8. Forward characteristics of reverse diode

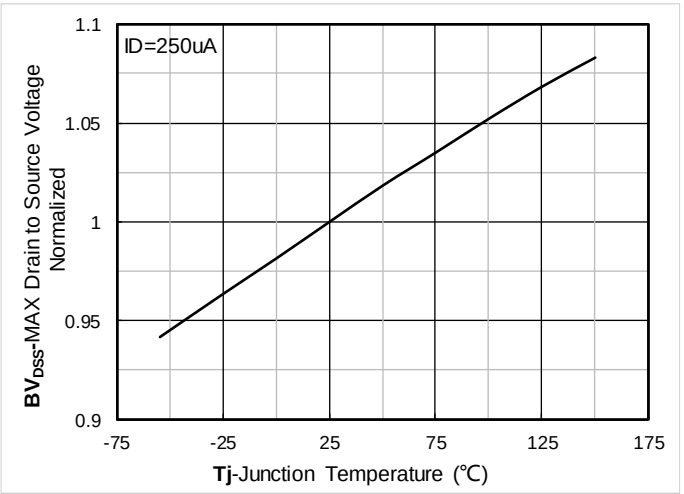


Figure 9. Normalized breakdown voltage

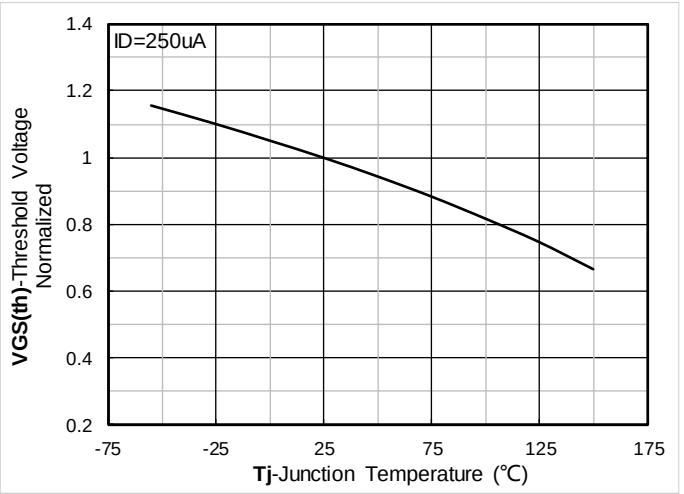


Figure 10. Normalized Threshold voltage

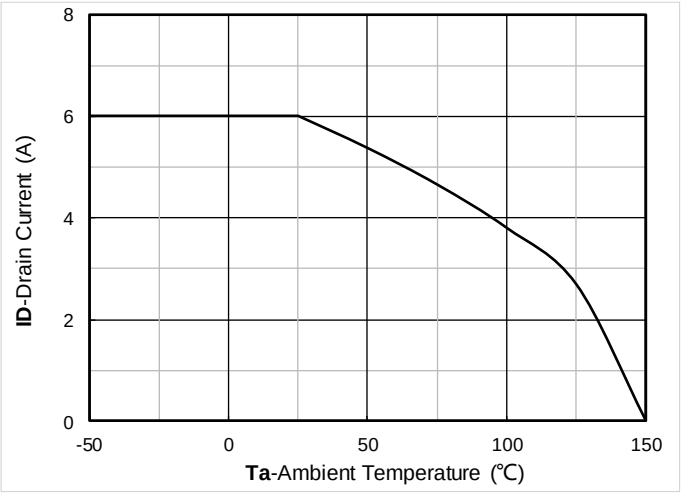


Figure 11. Current dissipation

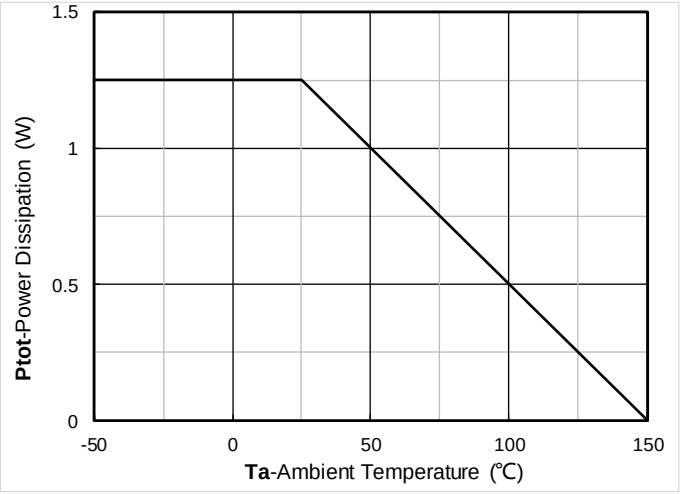


Figure 12. Power dissipation

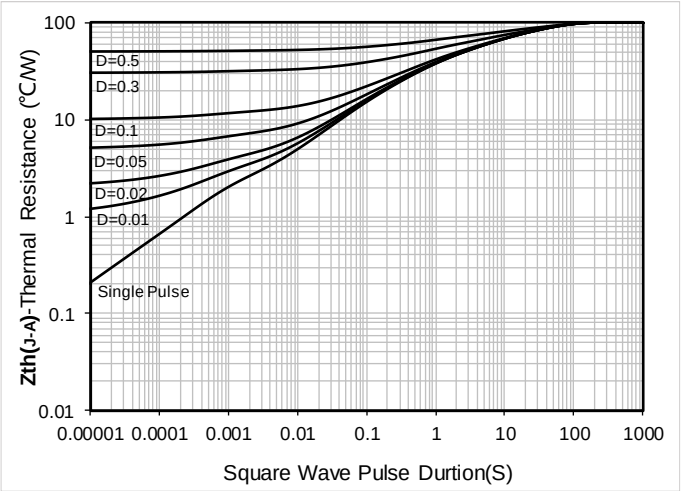


Figure 13. Maximum Transient Thermal Impedance

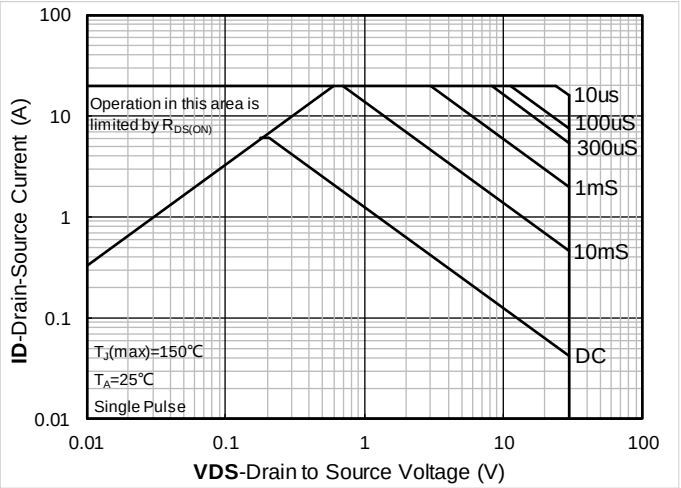


Figure 14. Safe Operation Area

■ PMOS Typical Electrical and Thermal Characteristics Diagrams

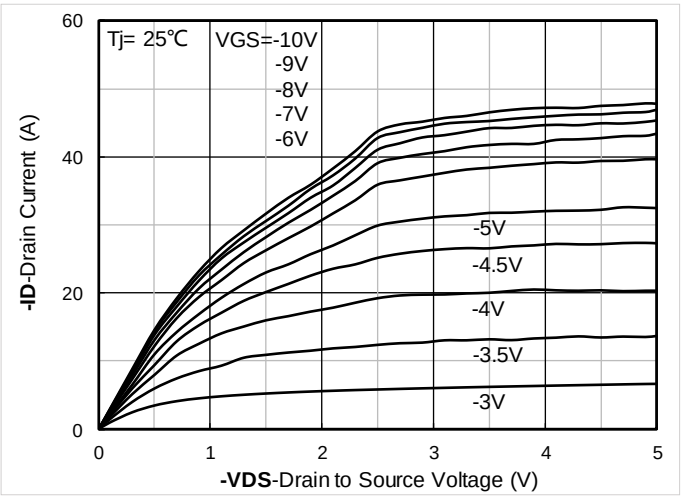


Figure 1. Output Characteristics

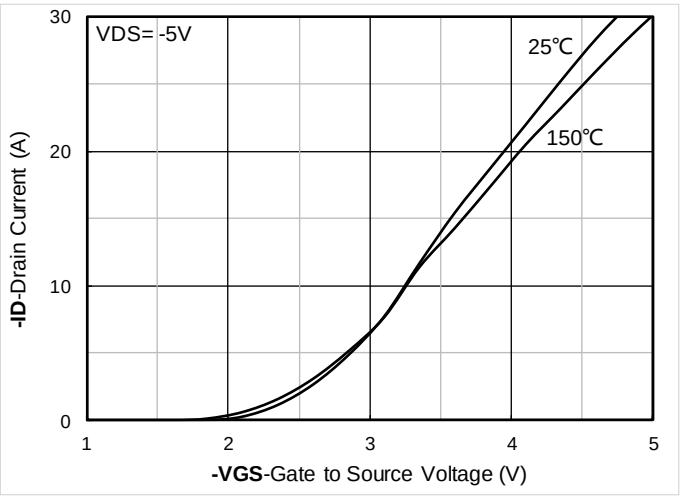


Figure 2. Transfer Characteristics

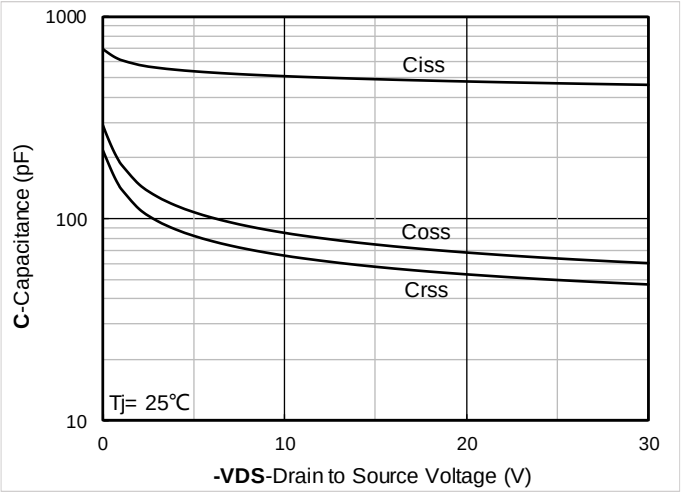


Figure 3. Capacitance Characteristics

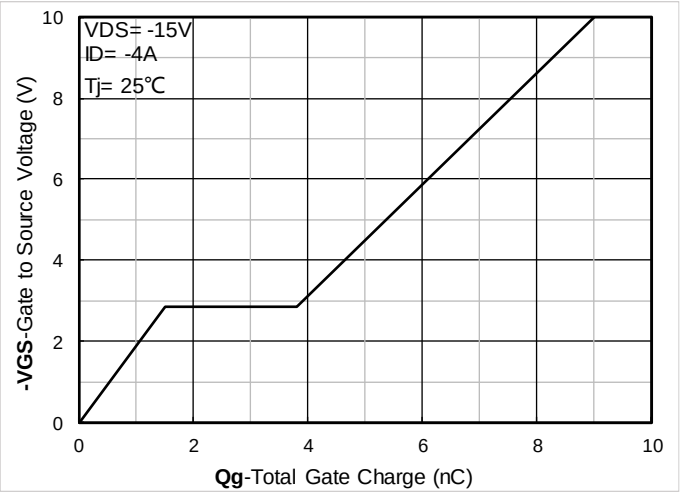


Figure 4. Gate Charge

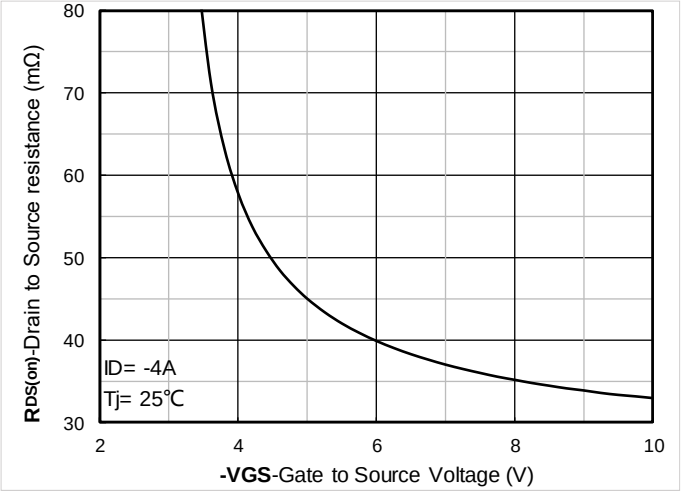


Figure 5. On-Resistance vs Gate to Source Voltage

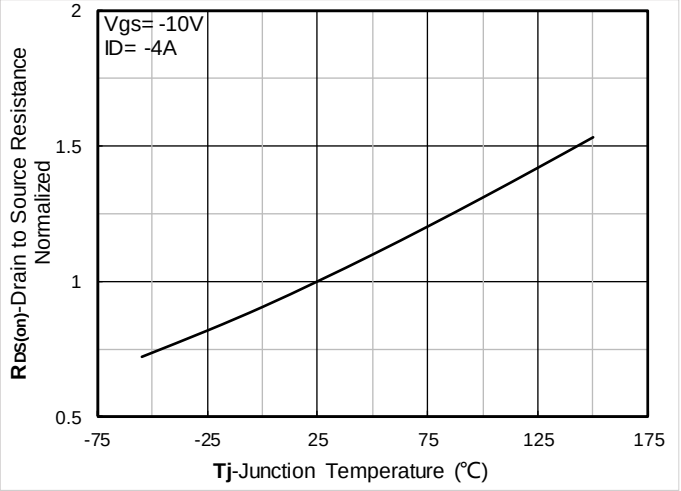


Figure 6. Normalized On-Resistance

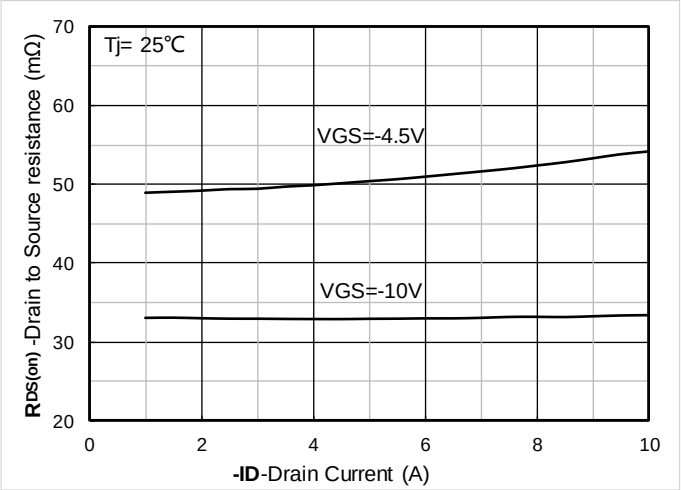


Figure 7. $R_{DS(on)}$ VS Drain Current

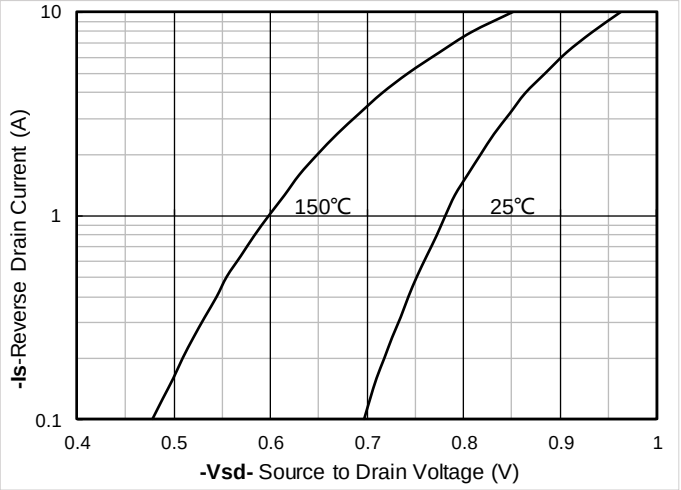


Figure 8. Forward characteristics of reverse diode

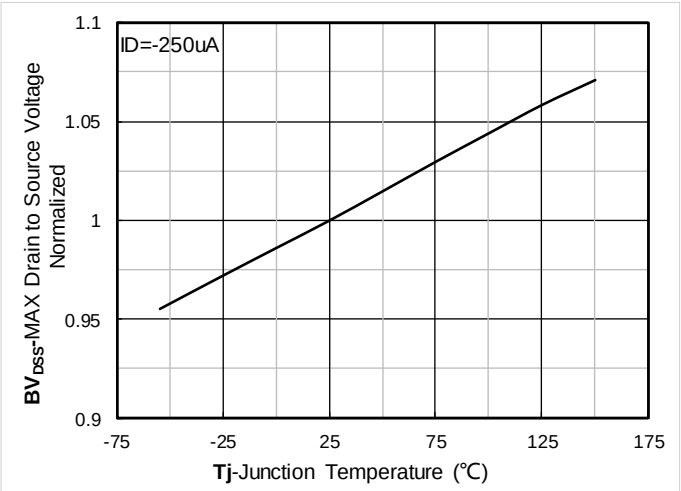


Figure 9. Normalized breakdown voltage

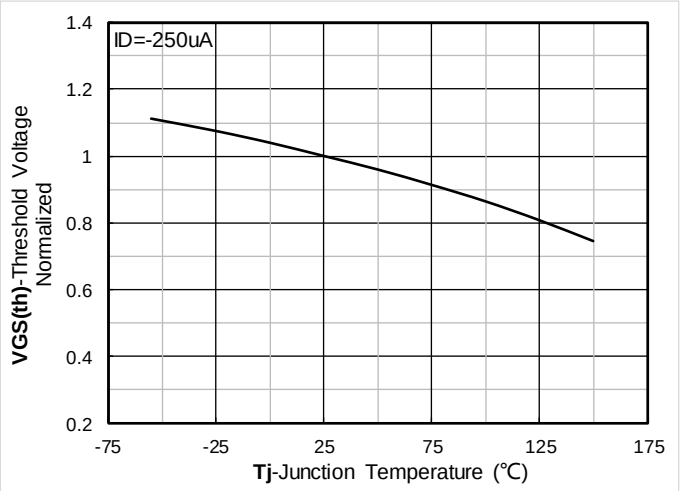


Figure 10. Normalized Threshold voltage

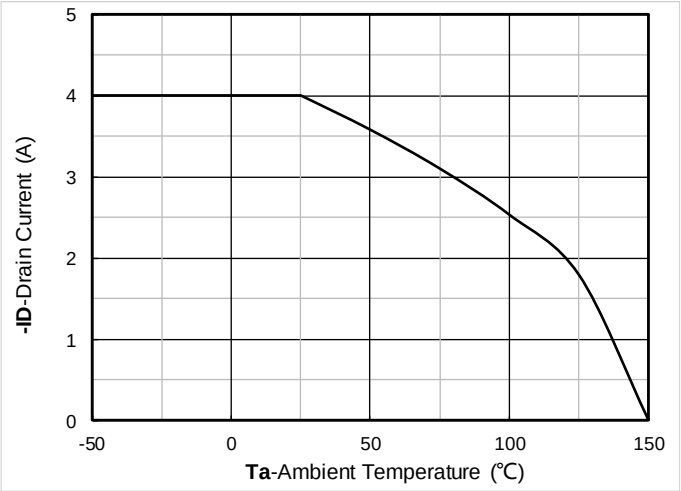


Figure 11. Current dissipation

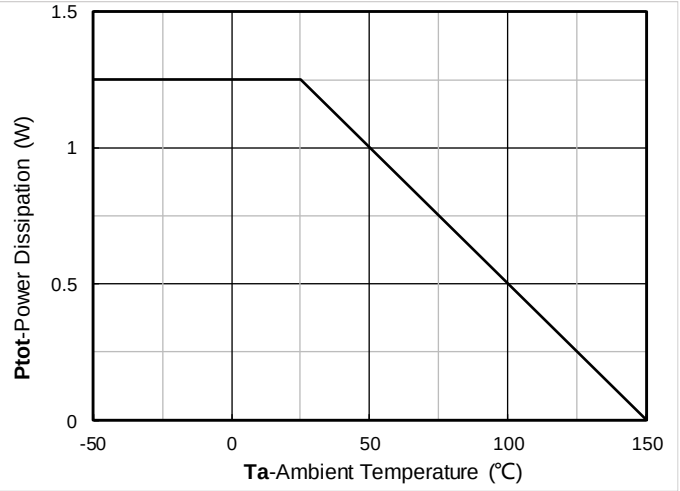


Figure 12. Power dissipation

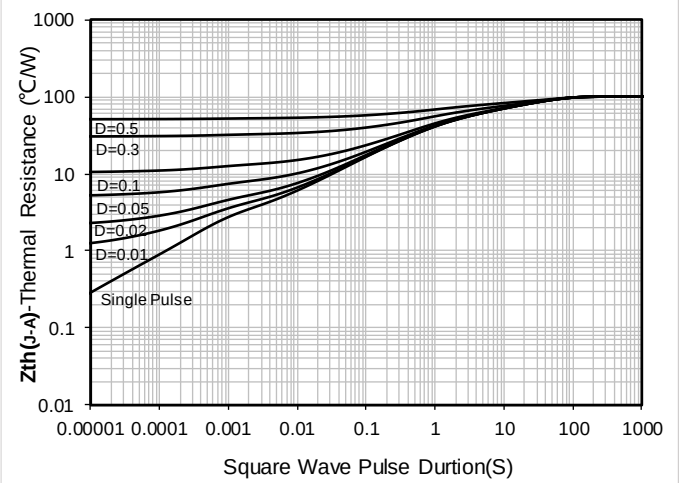


Figure 13. Maximum Transient Thermal Impedance

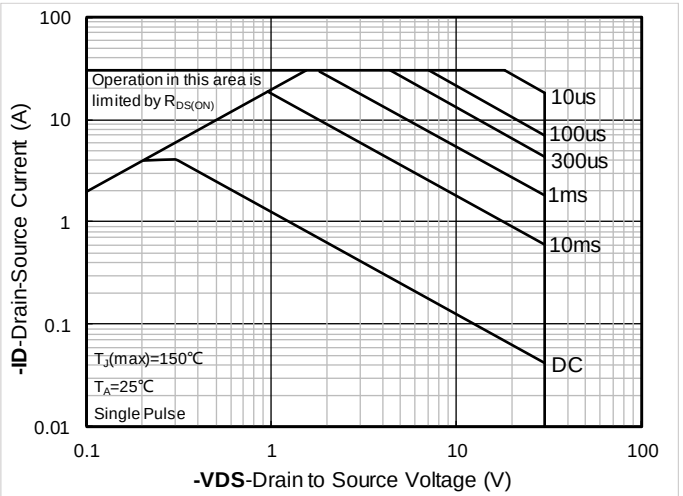
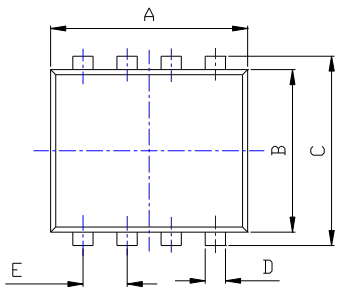
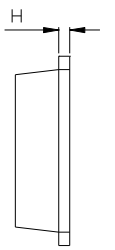


Figure 14. Safe Operation Area

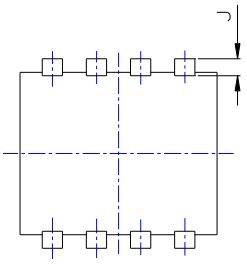
■ PDFN3030-8L Package information



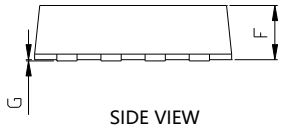
TOP VIEW



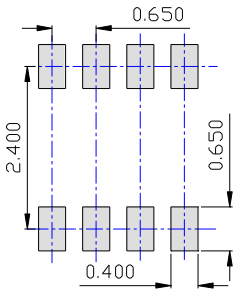
SIDE VIEW



BOTTOM VIEW



SIDE VIEW



SUGGESTED SOLDER PAD LAYOUT

UNIT：mm

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.108	0.120	2.750	3.050
B	0.089	0.100	2.250	2.550
C	0.104	0.116	2.650	2.950
D	0.008	0.016	0.200	0.400
E	0.026TYP		0.650TYP	
F	0.028	0.035	0.700	0.900
G	0.000	0.004	0.000	0.100
H	0.004	0.012	0.100	0.300
J	0.007	0.015	0.190	0.390

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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