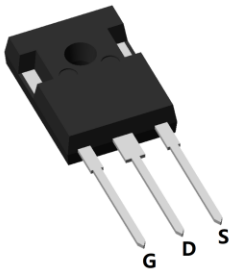
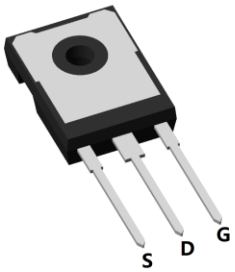
N-Channel Enhancement Mode Field Effect Transistor

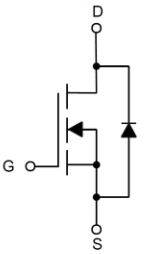


Top View



Bottom View

TO-247



Product Summary

- V_{DS} 150V
- I_D 149A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜5.9mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested
- ESD Level (HBM) H1C

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- UPS and Inverter applications
- Motor drivers
- DC-DC convertor

■ Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	150	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}= 10V	I_D	-	15	A
		T_A=100℃,V_{GS}= 10V		-	9.5	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}= 10V,Chip limitation		-	149	
		T_C=100℃,V_{GS}= 10V		-	94	
Pulsed Drain Current	T_C=25℃,t_p≤10μs		I_{DM}	-	596	
Maximum Body-Diode Continuous Current	T_C=25℃		I_S		149	
Avalanche energy (non-repetitive)	T_J=25℃,V_G=10V,R_G=25Ω,L=2mH,IAS=36.9A		EAS	-	1361	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	2.79	W
		T_A=100℃		-	1.11	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	271	
		T_C=100℃		-	108	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	150	℃

■Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	44.7	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	0.46	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
W5D9G15H	B1	W5D9G15H	30	360	1800	Tube

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA,Tj=25℃	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V,Tj=25℃	-	-	1	μA
		V_{DS}=150V,V_{GS}=0V,Tj=125℃	-	-	100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V,Tj=25℃	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA,Tj=25℃	2.2	3	3.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=50A,Tj=25℃	-	4.5	5.9	mΩ
Diode Forward Voltage	V_{SD}	I_S=50A,V_{GS}=0V,Tj=25℃	-	0.85	1.2	V
Gate Resistance	R_G	f=1MHz,Tj=25℃	-	1	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=75V,V_{GS}=0V,f=1MHz,Tj=25℃	-	4987	-	pF
Output Capacitance	C_{oss}		-	769	-	
Reverse Transfer Capacitance	C_{rss}		-	10.5	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=75V,I_D=50A,Tj=25℃	-	65.4	-	nC
Gate-Source Charge	Q_{gs}		-	23.2	-	
Gate-Drain Charge	Q_{gd}		-	9.7	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A,di/dt=100A/μs,V_{GS}=0V, V_R=75V,Tj=25℃	-	328	-	nC
Reverse Recovery Time	t_{rr}		-	111	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=75V,I_D=50A,R_{GEN}=3Ω, Tj=25℃	-	23.7	-	ns
Turn-on Rise Time	t_r		-	14.4	-	
Turn-off Delay Time	$t_{D(off)}$		-	40.4	-	
Turn-off Fall Time	t_f		-	13.5	-	

Note：
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured in the still air environment with T_A=25℃.The maximum allowed junction temperature of 150℃.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

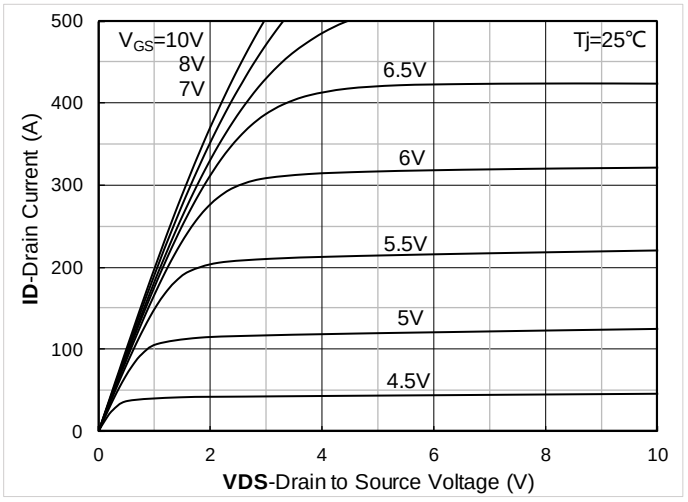


Figure 1. Output Characteristics; typical values

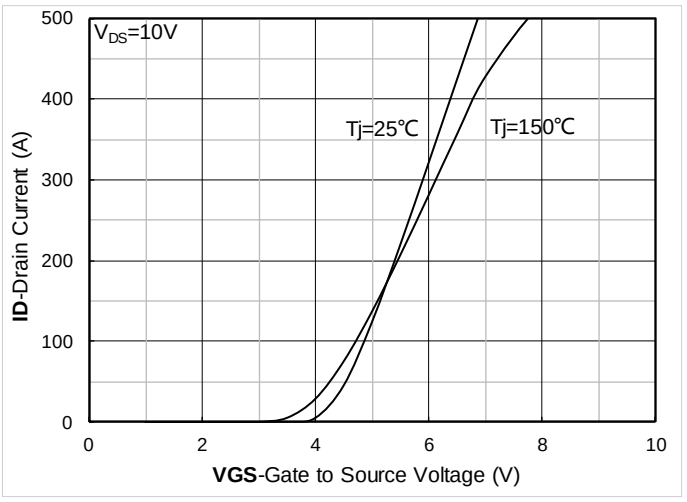


Figure 2. Transfer Characteristics; typical values

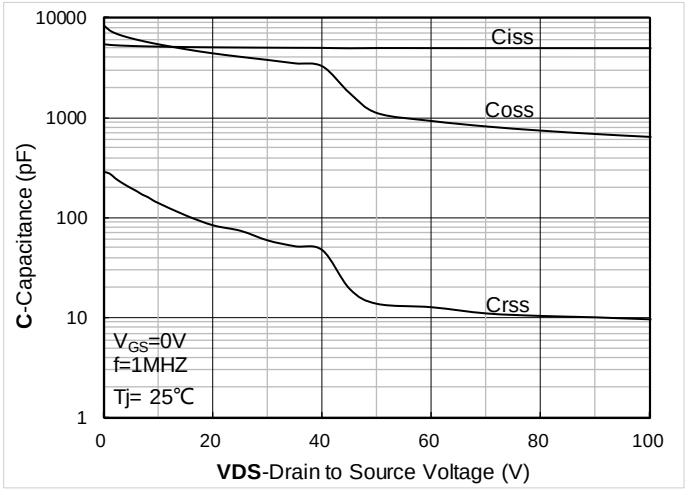


Figure 3. Capacitance Characteristics; typical values

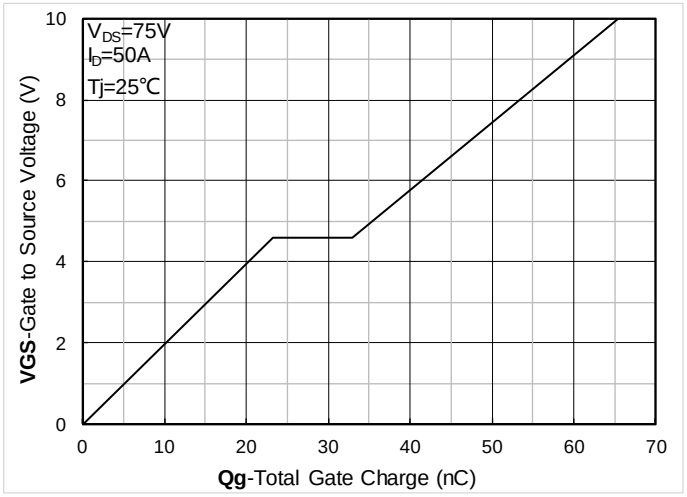


Figure 4. Gate Charge; typical values

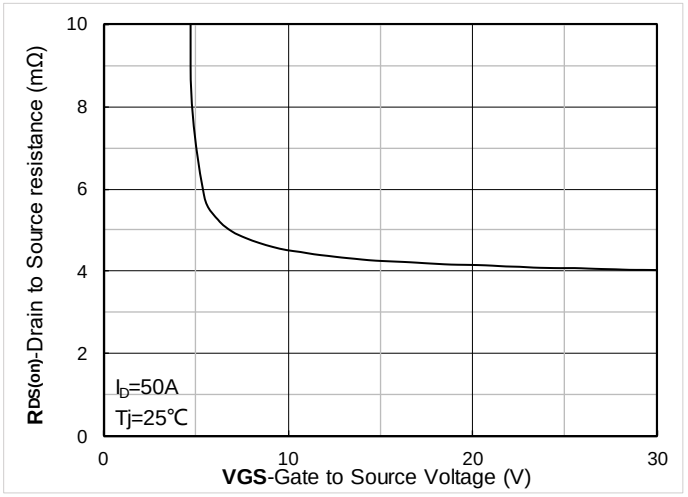


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

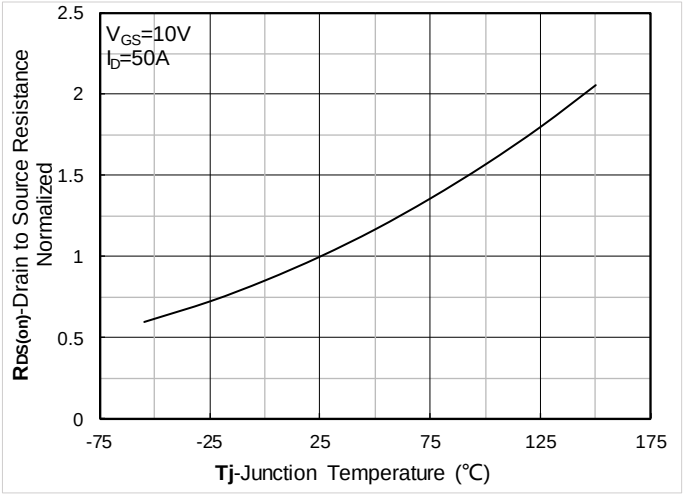


Figure 6. Normalized On-Resistance

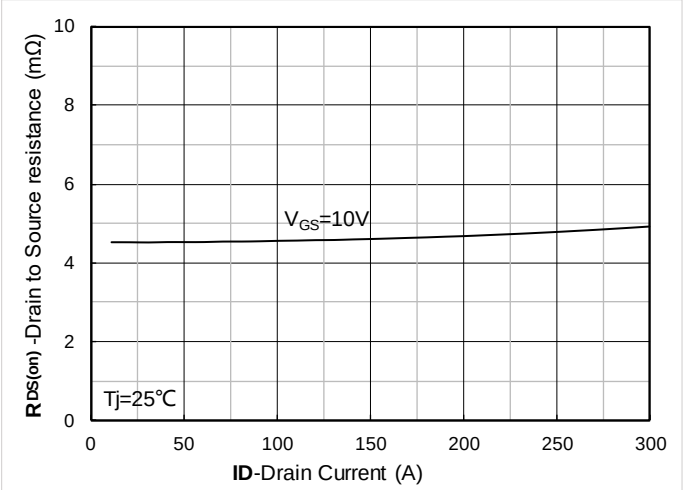


Figure 7. $R_{DS(on)}$ VS Drain Current; typical values

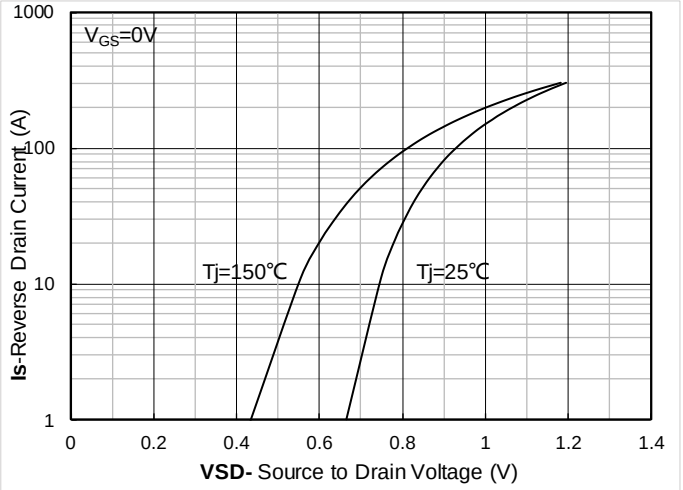


Figure 8. Forward characteristics of reverse diode; typical values

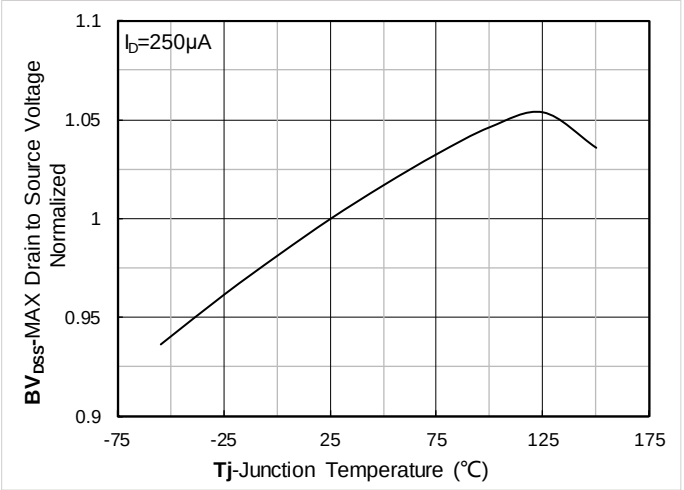


Figure 9. Normalized breakdown voltage

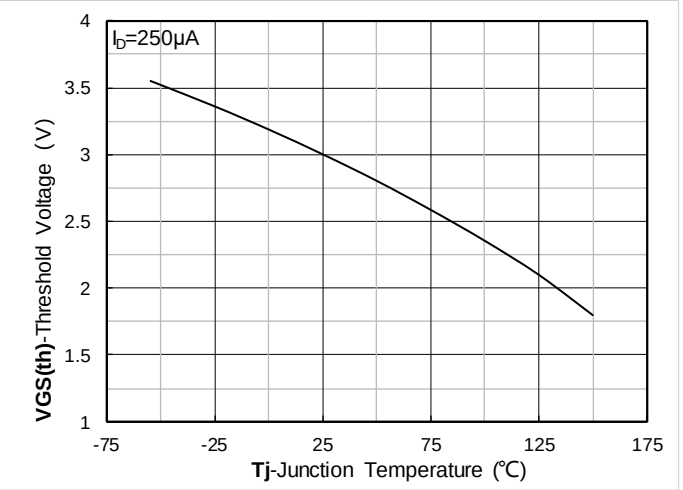


Figure 10. Gate threshold voltage; typical values

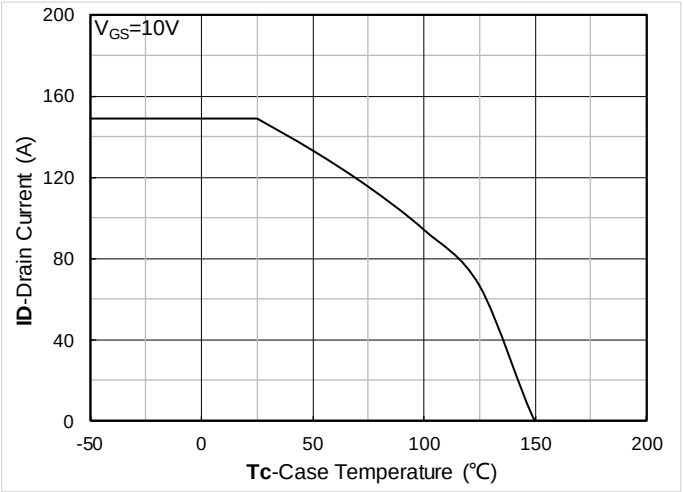


Figure 11. Current dissipation

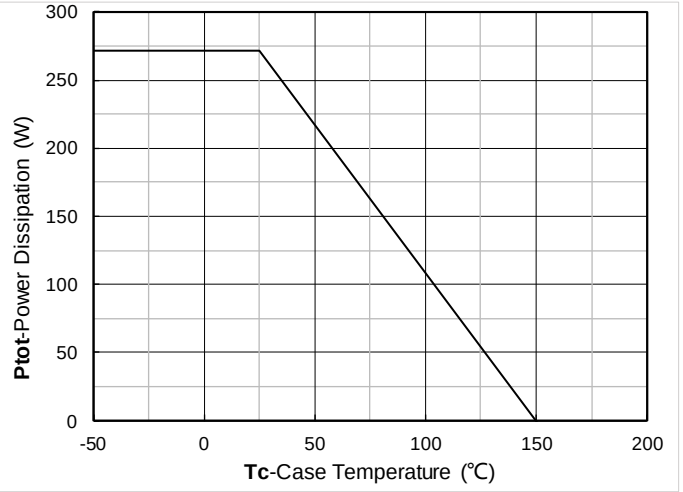


Figure 12. Power dissipation

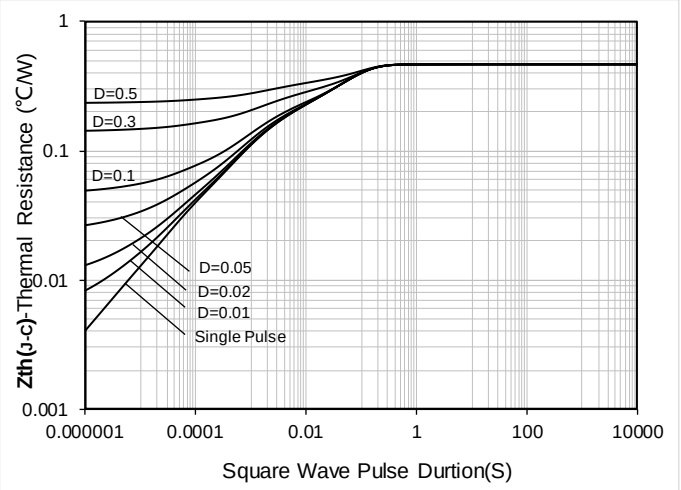


Figure 13. Maximum Transient Thermal Impedance

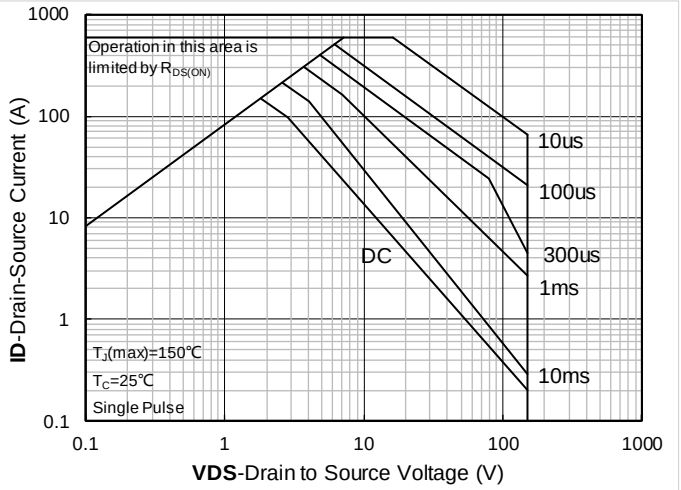
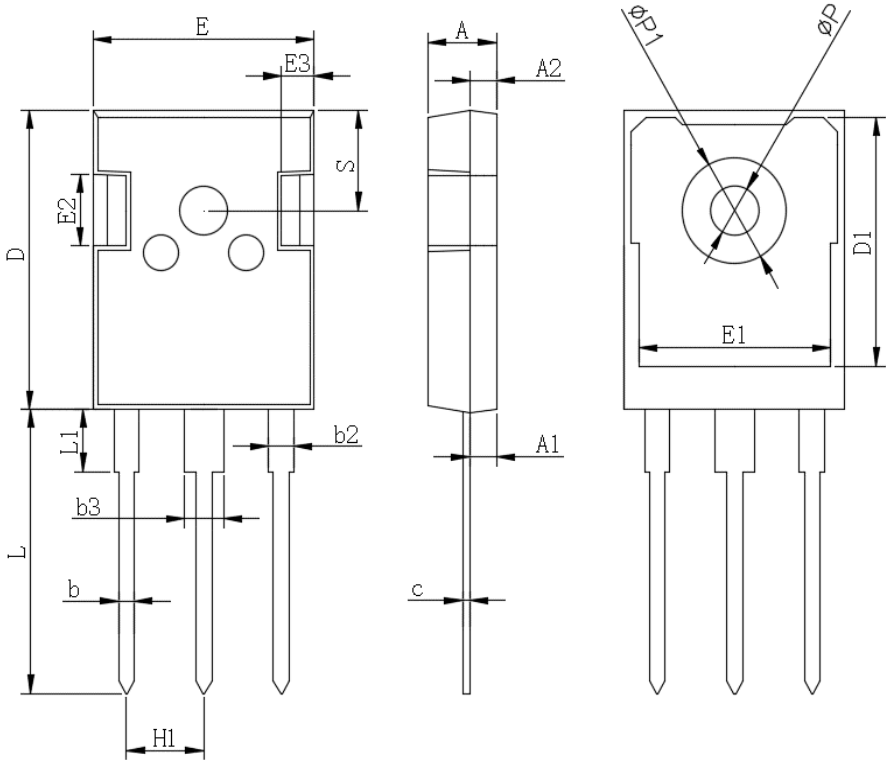


Figure 14. Safe Operation Area

■ TO-247AB Package information

TO-247AB



TO-247AB		
Dim	Min	Max
A	4.80	5.20
A1	2.21	2.61
A2	1.85	2.15
b	1.0	1.4
b2	1.91	2.21
c	0.5	0.7
D	20.70	21.30
D1	16.25	16.85
E	15.50	16.10
E1	13.0	13.6
E2	4.80	5.20
E3	2.30	2.70
L	19.62	20.22
L1	-	4.30
ΦP	3.40	3.80
ΦP1	-	7.30
S	6.15TYP	
H1	5.44TYP	
b3	2.80	3.20

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