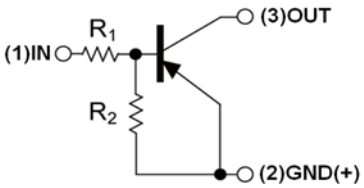
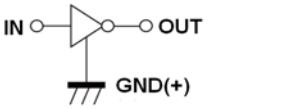
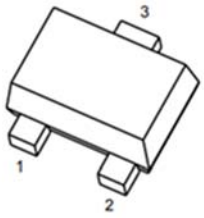
PNP Digital Transistors (Built-in Resistors)







1. IN
2. GND
3. OUT

SOT-723

Features

- Moisture sensitivity level 1
- Halogen free and RoHS compliant
- Surface mount package ideally suited for auto matic insertion.

Application

- Signal amplification
- Switching circuit

Mechanical data

- **Package**: SOT-723
- **Terminals**: Tin plated leads, solderable per J-STD-002 and JESD22-B102

■ **Maximum Ratings** (T_a=25℃ Unless otherwise specified)

Item	Symbol	Unit	Conditions	Value
Device marking code				14
Supply voltage	V_{CC}	V		-50
Input voltage	V_{IN}	V		-40 to 10
Output current	I_O	mA		-100
Power dissipation	P_D	mW		100
Junction temperature	T_J	℃		-55 to +150
Storage temperature	T_{STG}	℃		-55 to +150

■ Electrical Characteristics (Ta=25℃ Unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Input voltage	$VI_{(off)}$	V	V_{CC}=-5V,I_O=-100uA	-0.5		
	$VI_{(on)}$	V	V_O=-0.3V,I_O=-10mA			-3
Output voltage	$V_{O\ (on)}$	V	I_O /I_I =-10mA/-0.5 mA			-0.3
Input current	I_I	mA	V_I=-5V			-0.88
Output current	$I_{O(off)}$	uA	V_{CC}=-50V, V_I=0			-0.5
DC current gain	G_I		V_O=-5V, Io =-5mA	30		
Input resistance	R_1	kΩ		7	10	13
Resistance ratio	R_2/R_1			0.8	1	1.2
Transition frequency	f_T	MHz	V_O=-10V,I_O=-5mA,f=100MHz		250	

■ Thermal Characteristics

Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	$R_{\theta J\text{-}A}$(1)	℃/W	1250
Thermal resistance, junction-to-case	$R_{\theta J\text{-}C}$(1)	℃/W	1000

Note: Thermal resistance from junction to ambient and from junction to case mounted on P.C.B. with 25.4mm*25.4mm copper pad areas

■Ordering Information

Preferred P/N	Packing code	Unit weight(g)	Minimum package(pcs)	Inner box quantity(pcs)	Outer carton quantity(pcs)	Delivery mode
DTA114EM	F2	Approximate 0.0013	8000	80000	320000	7” reel

■Characteristics

Fig 1：DC Current Gain Characteristics

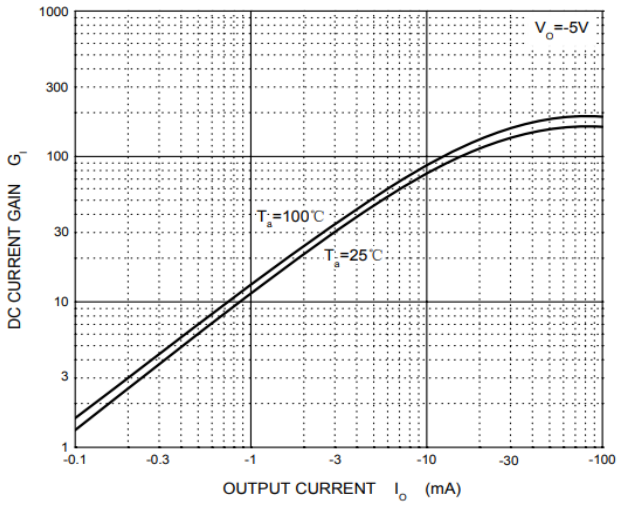


Fig 2：Input Voltage (On) Characteristics

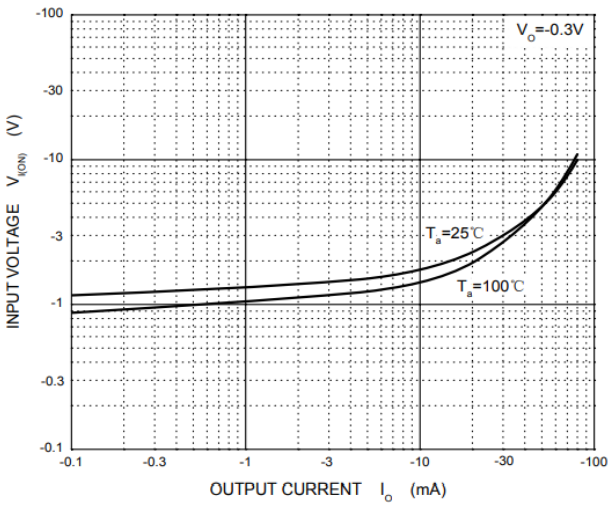


Fig 3：Input Voltage (Off) Characteristics

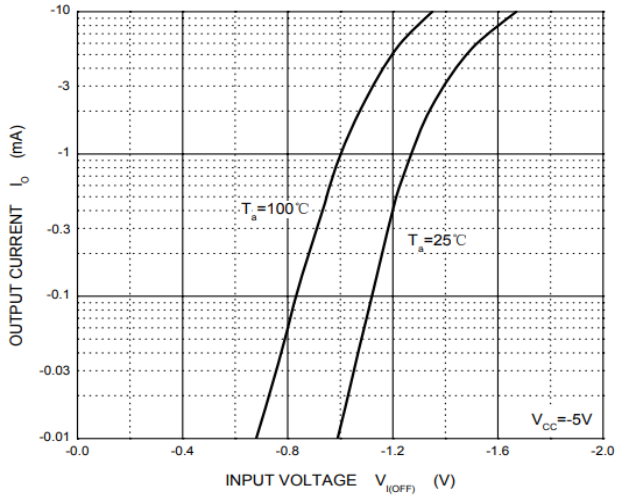


Fig 4：Output Voltage Characteristics

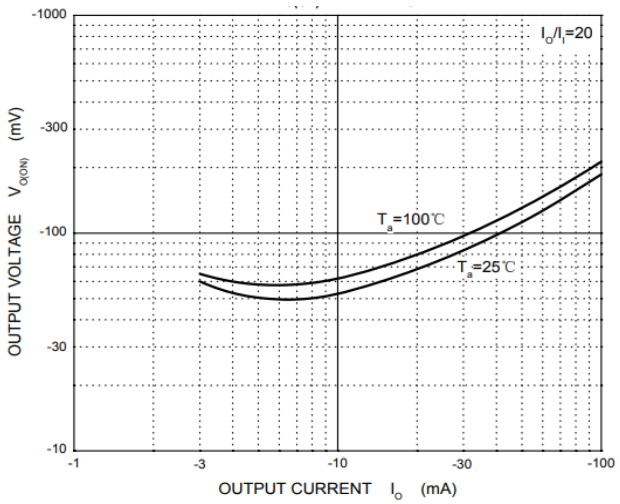
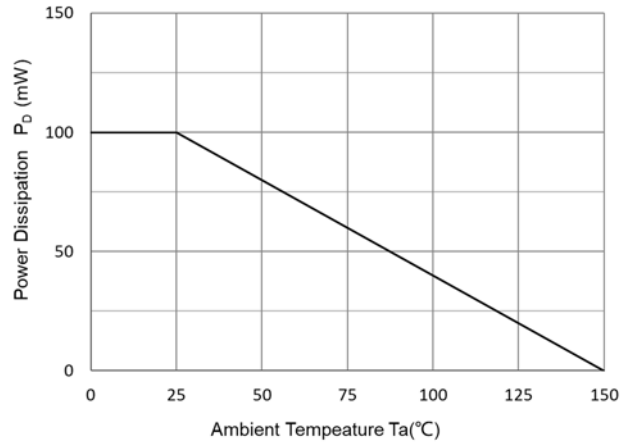
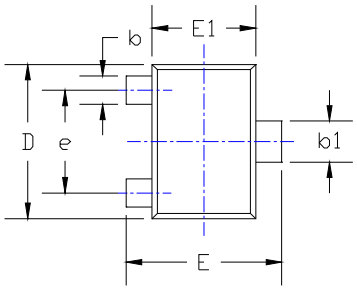


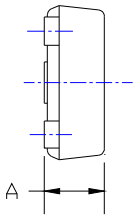
Fig 5：P_D-Ta Curve



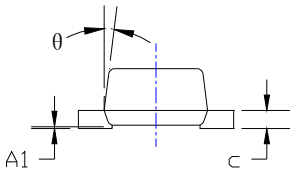
■ Outline Dimensions



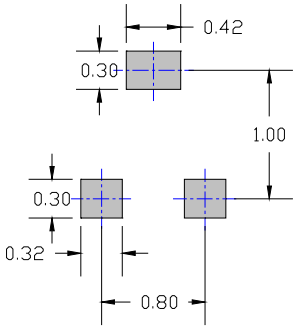
TOP VIEW



SIDE VIEW



SIDE VIEW



SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.017	0.022	0.430	0.550
A1	0.000	0.002	0.000	0.050
b	0.007	0.011	0.170	0.270
b1	0.011	0.015	0.270	0.370
c	0.003	0.008	0.080	0.200
D	0.045	0.049	1.150	1.250
E	0.045	0.049	1.150	1.250
E1	0.030	0.033	0.750	0.850
e	0.031TYP.		0.800TYP.	
θ	7°REF.		7°REF.	

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:
1. All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位，除非另有说明]
2. General tolerances: ±0.10mm unless otherwise specified.
[通用公差为±0.10mm，除非另有说明]
3. Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
4.All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
5.Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
6.Dimensions D and E1are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸]
7.Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面，共面性最大为0.1mm]
8. ★It is the key size.
[★ 标记为关键尺寸]

Notice

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