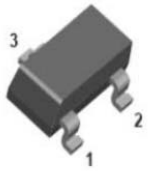
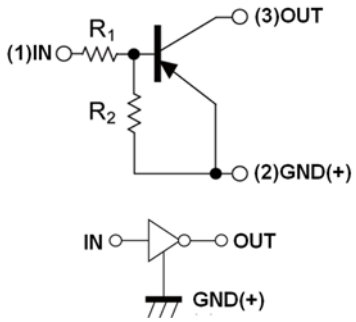
PNP Digital Transistors (Built-in Resistors)



1. IN
2. GND
3. OUT

SOT-23



Features

- Moisture sensitivity level 1
- Halogen free and RoHS compliant
- Surface mount package ideally suited for automatic insertion

Application

- Signal amplification
- Switching circuit

Mechanical data

- **Package**: SOT-23
- **Terminals**: Tin plated leads, solderable per J-STD-002 and JESD22-B102

■ Maximum Ratings (T_a=25℃ Unless otherwise specified)

Item	Symbol	Unit	Conditions	Value
Device marking code				F21
Supply voltage	V_{CC}	V		-50
Input voltage	V_{IN}	V		-10 to +5
Output current	I_O	mA		-100
Power dissipation	P_D	mW		200
Junction temperature	T_J	℃		-55 to +150
Storage temperature	T_{STG}	℃		-55 to +150

■ Electrical Characteristics (Ta=25℃ Unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Collector-emitter cut-off current	I_{CEO}	nA	V_{CE}=-50V, I_B=0			-500
Collector-base cut-off current	I_{CBO}	nA	V_{CB}=-50V, I_E=0			-100
Emitter-base cut-off current	I_{EBO}	uA	V_{EB}=-6V, I_C=0			-2500
Collector-base breakdown voltage	$V_{(BR)CBO}$	V	I_C=-100μA, I_E=0	-50		
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	V	I_C =-2mA, I_B=0	-50		
Emitter-base breakdown voltage	$V_{(BR)EBO}$	V	I_E=-2mA, I_C=0	-6		
Collector-emitter saturation voltage	$V_{CE(SAT)}$	V	I_C /I_B =-10mA/-5mA			-0.25
DC current gain	h_{FE}		V_{CE}=-10V, Ic =-20mA	30		
Input resistance	R_1	kΩ		1.5	2.2	2.9
Resistance ratio	R_2/R_1			0.8	1	1.2
Transition frequency	f_T	MHz	V_O=-10V,I_O=-5mA,f=100MHz		250	

■ Thermal Characteristics

Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	$R_{\theta J-A}$(1)	℃/W	625
Thermal resistance, junction-to-case	$R_{\theta J-C}$(1)	℃/W	500

Note:

（1）Device mounted on PCB, single-sided copper， with standard footprint

■Ordering Information

Preferred P/N	Packing code	Unit weight(g)	Minimum package(pcs)	Inner box quantity(pcs)	Outer carton quantity(pcs)	Delivery mode
DTA123ECA	F2	Approximate 0.009	3000	30000	120000	7” reel

■Characteristics

Fig. 1 - DC Current Gain Characteristics

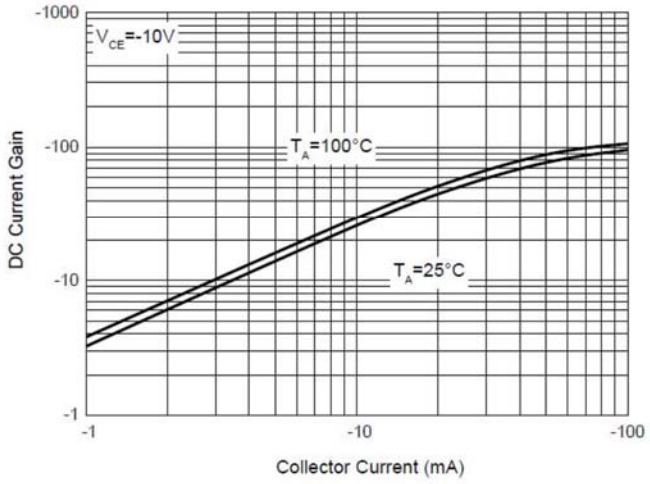


Fig. 2 - Collector-Emitter Saturation Voltage Characteristics

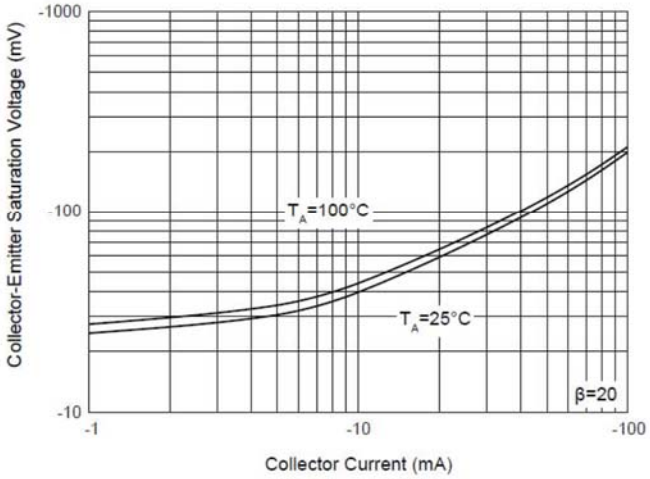
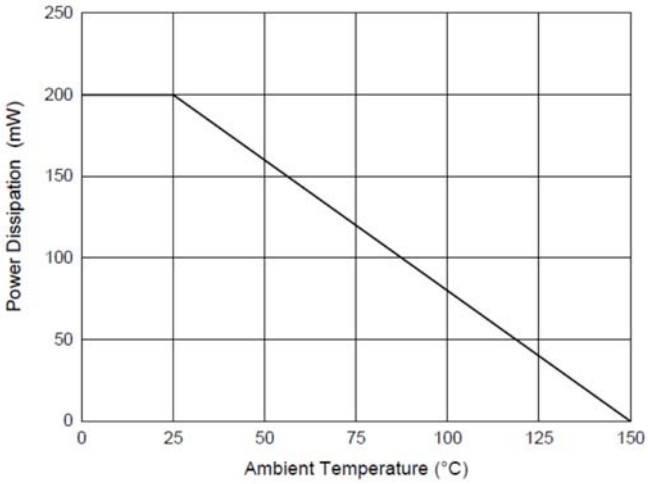
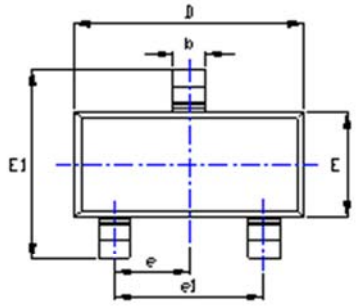


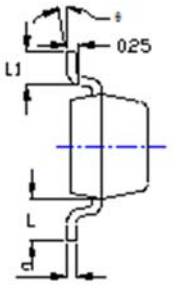
Fig. 3 - Power Derating Curve



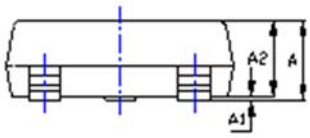
■ Outline Dimensions



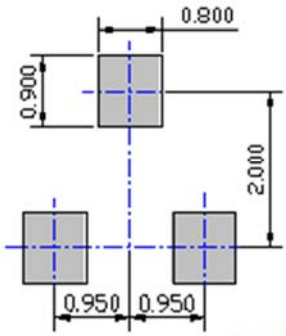
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:
1. All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位，除非另有说明]
2. General tolerances: ±0.10mm unless otherwise specified.
[通用公差为±0.10mm，除非另有说明]
3. Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
4.All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
5.Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
6.Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸]
7.Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面，共面性最大为0.1mm]
8. ★It is the key size.
[★ 标记为关键尺寸]

Notice

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