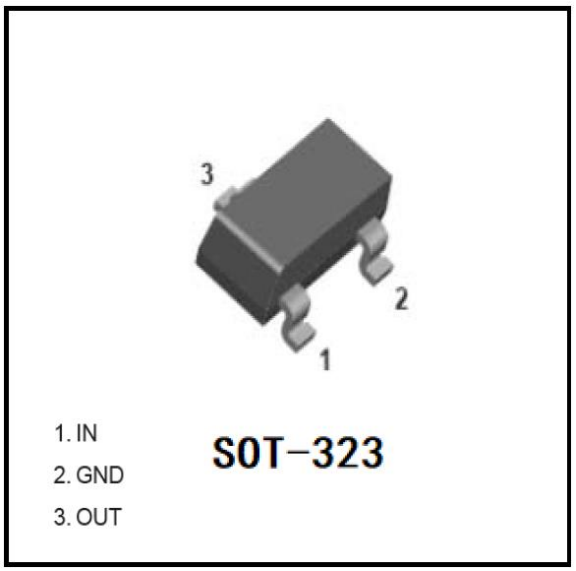
Digital Transistors (Built-in Resistors)



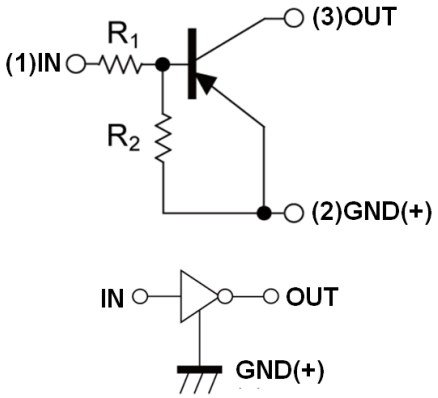
Features

- Epoxy meets UL-94 V-0 flammability rating
- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors
- Surface mount package ideally Suited for Automatic Insertion
- PNP

Mechanical Data

- **Package:** SOT-323
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Marking:** 13

■Equivalent circuit



■Maximum Ratings (Ta=25℃ Unless otherwise specified)

ITEM	SYMBOL	UNIT	CONDITIONS	VALUE
Supply Voltage	V_{CC}	V		-50
Input Voltage	V_{IN}	V		-30 to +10
Output Current	I_O	mA		-100
Power Dissipation	P_D	mW		200
Junction Temperature	Tj	℃		-55 to +150
Storage Temperature	T_{STG}	℃		-55 to +150

■Electrical Characteristics (Ta=25℃ unless otherwise specified)

ITEM	SYMBOL	UNIT	CONDITIONS	MIN	TYP	MAX
Input voltage	$VI_{(off)}$	V	V_{CC}=-5V, I_C=-100uA	-0.5		
	$VI_{(on)}$	V	V_O=-0.3V, I_C=-20mA			-3
Output voltage	$Vo_{(on)}$	V	I_O/I_I =-10mA/-0.5mA			-0.3
Input current	II	mA	VI=-5V			-1.8
Output current	$I_{O(off)}$	uA	V_{CC}=-50V, VI=0			-0.5
DC current gain	GI		V_O=-5V, I_O=-10mA	30		
Input resistance	R_1	kΩ		3.29	4.7	6.11
Resistance ratio	R_2/R_1			0.8	1.0	1.2
Transition frequency	f_T	MHz	V_{CE}=-10V, I_E=5mA, f=100MHz		250	

■ Thermal Characteristics

Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	$R_{\theta J\text{-}A}$(1)	℃/W	625
Thermal resistance, junction-to-case	$R_{\theta J\text{-}C}$(1)	℃/W	500

Note: Device mounted on PCB, single-sided copper，with standard footprint.

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	UNIT WEIGHT(g)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
DTA143EUA	F2	Approximate 0.006	3000	30000	120000	7” reel

■ **Characteristics** (Typical)

Fig. 1 - DC Current Gain Characteristics

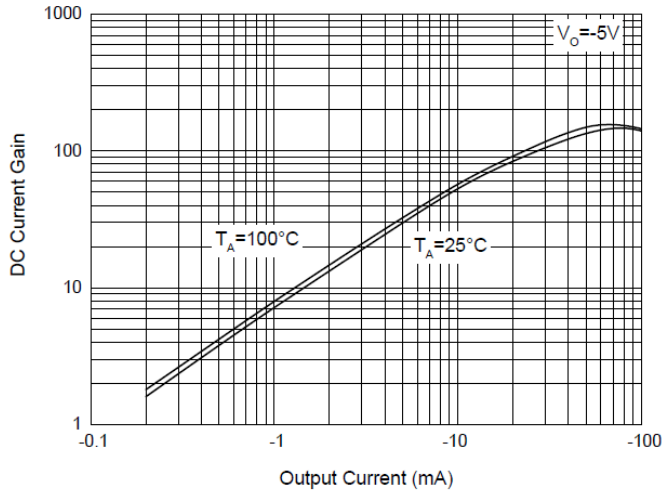


Fig. 2 - Input Voltage (on) Characteristics

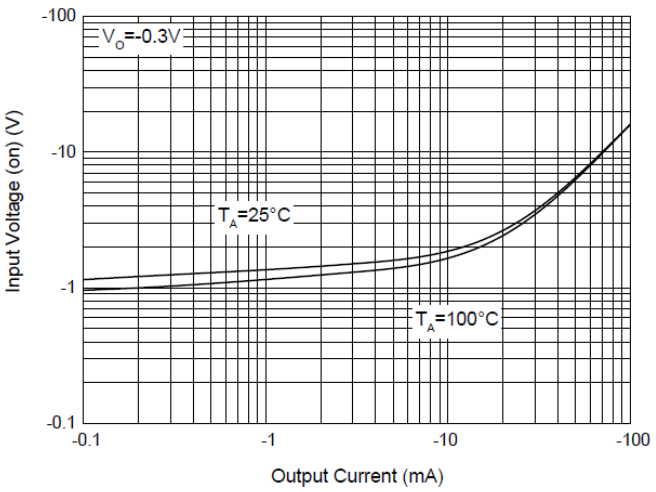


Fig. 3 - Input Voltage (off) Characteristics

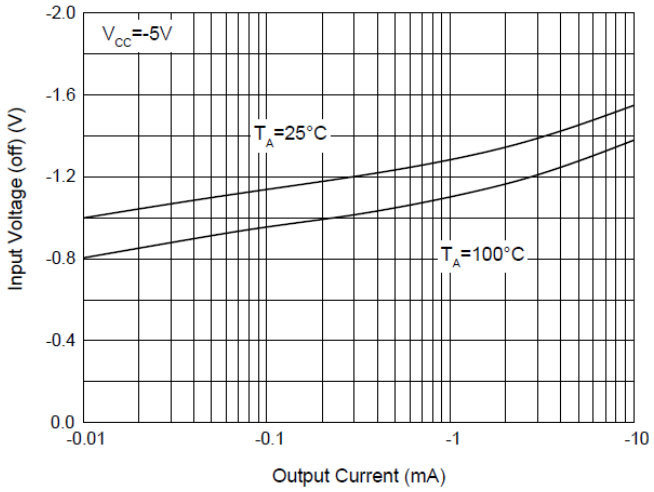
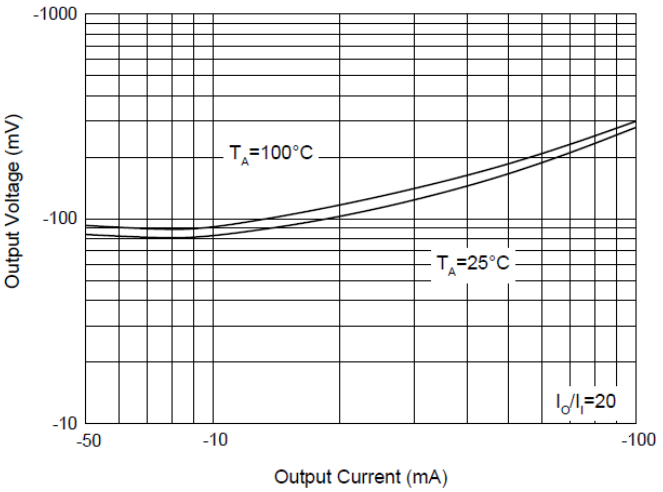
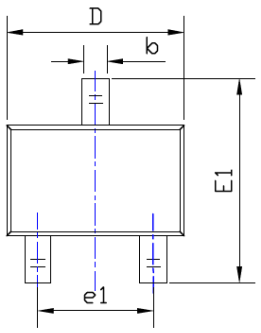


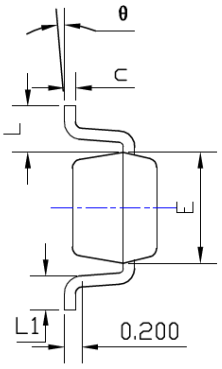
Fig. 4 - Output Voltage Characteristics



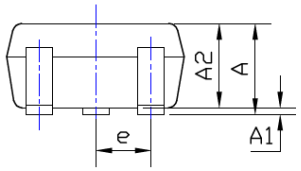
■SOT-323 Package Outline Dimensions



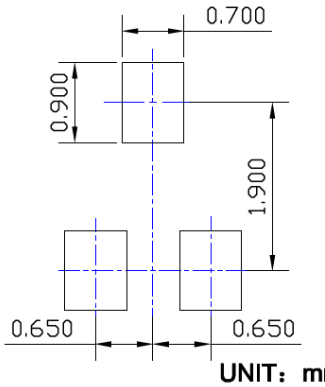
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT：mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.043	0.900	1.100
A1	0.000	0.004	0.000	0.100
A2	0.035	0.039	0.900	1.000
b	0.006	0.016	0.150	0.400
c	0.004	0.010	0.100	0.250
D	0.071	0.087	1.800	2.200
E	0.045	0.053	1.150	1.350
E1	0.085	0.096	2.150	2.450
e	0.026TYP		0.650TYP	
e1	0.047	0.055	1.200	1.400
L	0.021REF		0.525REF	
L1	0.010	0.018	0.260	0.460
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:
1. All dimensions are in millimeters (mm) unless otherwise specified.
[所有尺寸均以毫米为单位，除非另有说明]
2. General tolerances: ±0.10mm unless otherwise specified.
[通用公差为±0.10mm，除非另有说明]
3. Dimensions and tolerances per ASME Y14.5M-2018.
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
4.All dimensions shown are exclusive of burrs and gate residues.
Burrs and gate vestiges shall not exceed 0.15 mm in maximum.
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
5.Dimension b does not include dambar protrusion of max 0.100 mm per side.
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
6.Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.
[D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸]
7.Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.
[成型的管脚应为同一平面，共面性最大为0.1mm]
8. ★It is the key size.
[★ 标记为关键尺寸]

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